

10GBASE-LX4-C

Enterasys® 10GBASE-LX4 Compatible TAA Compliant 10GBase-LX4 XENPAK Transceiver (MMF, 1310nm, 300m, SC)

Features:

- INF-8474 Compliance
- Duplex SC Connector
- Single-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free



Applications:

- 10GBase Ethernet
- Access and Enterprise

Product Description

This Enterasys® 10GBASE-LX4 compatible XENPAK transceiver provides 10GBase-LX4 throughput up to 300m over multi-mode fiber (MMF) using a wavelength of 1310nm via a SC connector. It is guaranteed to be 100% compatible with the equivalent Enterasys® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. It is built to meet or exceed the specifications of Enterasys®, as well as to comply with MSA (Multi-Source Agreement) standards to ensure seamless network integration. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")



Absolute Maximum Ratings

| Parameter | | Symbol | Min. | Тур. | Max. | Unit | Notes |
|-----------------------------------|----------------------------|--------|-------|---------|--------|------|-------|
| Storage Ambient Temperature Range | | Tstg | -40 | | +85 | °C | |
| Powered Case Ten | nperature Range | | | | +70 | °C | |
| Supply Voltage AP | S | Vaps | | | 1.5 | V | |
| Supply Voltage Ra | nge @ 3.3V | Vcc3 | -0.5 | | 4.0 | V | |
| Operating Case Te | Operating Case Temperature | | | | +70 | °C | |
| Power Supply Volt | Power Supply Voltage | | 3.13 | 3.3 | 3.47 | V | |
| | | | 1.152 | 1.2 | 1.248 | | |
| Power Dissipation | | PD | | 3.5 | 4 | W | |
| Operating Range | Single-Mode Fiber | Lop | 2 | | 10,000 | m | |
| Data Rate | 10GBASE-LR Module | DR | | 10.3125 | | Gbps | |

Electrical DC Characteristics

| Parameter | Symbol | Min. | Тур. | Max. | Unit | Notes | | |
|---|------------|------|------|------|------|-------|--|--|
| 1.2V CMOS (1.8V CMOS Compatible) I/O DC Characteristics (PRTAD;LASI;RESET;TX_ONOFF) | | | | | | | | |
| Output High Voltage | VOH | 1 | | | V | 1 | | |
| Output Low Voltage | VOL | | | 0.15 | V | | | |
| Input High Voltage | VIH | 0.84 | | 1.5 | V | | | |
| Input Low Voltage | VIL | | | 0.36 | V | | | |
| Input Pull-Down Current | IPD | 20 | | 120 | uA | | | |
| XAUI I/O DC Characteristics (TXLANE[03]; R. | XLANE[03]) | | | | | | | |
| Differential Input Amplitude (Pk-Pk) | | 220 | | 1600 | mV | 4 | | |
| Differential Output Amplitude (Pk-Pk) | | 800 | | 1600 | | 4 | | |
| MDIO I/O DC Characteristics (MDIO; MDC) | | | | | | | | |
| Output Low Voltage | VOL | -0.3 | | 0.2 | V | | | |
| Output Low Current | IOL | | | 20 | mA | | | |
| Input High Voltage | VIH | 0.84 | | 1.5 | V | | | |
| Input Low Voltage | VIL | -0.3 | | 0.36 | V | | | |

Notes:

- 1. For 1.8V CMOS, VOH=1.65V (minimum), VOL=0.15V (maximum), VIH=1.17V (minimum), and VIL = 0.63V (maximum).
- 2. Rpull-up= $10k\Omega$ to 1.86V.
- 3. VIN=1.8V.
- 4. AC coupled.

Electrical AC Characteristics

| Parameter | Symbol | Min. | Тур. | Max. | Unit | Notes |
|---|--------|---------------|----------------|----------------|------|-------|
| XAUI Input AC Characteristics (TXLANE[03]) | | | | | | |
| XAUI Baud Rate | DRin | | 3.125 | | Gbps | |
| Differential Input Impedance | ZIN | 80 | 100 | 120 | Ω | |
| XAUI Output AC Characteristics (RXLANE[03]) | | | | | | |
| XAUI Baud Rate | DRout | | 3.125 | | Gbps | |
| XAUI Eye Mask (Far-End) | | Accord | ing to IEEE 80 |)2.3ae | | 3 |
| Output Differential Impedance | ZO | 80 | 100 | 120 | Ω | |
| Total Jitter | TJXAUI | | | 0.35 | UI | 4 |
| Deterministic Jitter | DJXAUI | | | 0.37 | UI | 4 |
| Power-On Reset AC Characteristics | | | | | | |
| Power-On Reset AC Characteristics | Acco | rding to XENI | PAK MSA Issu | ie 3.0, 2002-9 | 9-18 | |
| MDIO I/O AC Characteristics (MDIO; MDC) | | | | | | |
| MDIO Data Hold Time | tHOLD | 10 | | | ns | |
| MDIO Data Set-Up Time | tSU | 10 | | | ns | |
| Delay from MDC Rising Edge to MDIO Data Change | tDELAY | | | 300 | ns | 2 |
| MDC Clock Rate | fMAX | | | 2.5 | MHz | 1 |

Notes:

- 1. 100MHz to 2.5GHz.
- 2. At crossing point.
- 3. Per IEEE Std 802.3ae.
- 4. At near-end, no pre-equalization, 1UI = 320ps.

Optical Characteristics

| Parameter | Symbol | Min. | Тур. | Max. | Unit | Notes |
|---|--------|---------|---------------|-------|-------|-------|
| Transmitter | | | | | | |
| Average Launch Power | Pavg | -8.2 | | -0.5 | dBm | |
| Transmitter and Dispersion Penalty | TDP | | | 3.2 | dB | |
| Center Wavelength Range | λ | 1260 | 1310 | 1355 | nm | |
| Side-Mode Suppression Ratio | SMSR | 30 | | | dB | |
| Extinction Ratio | ER | 4.0 | 6 | | dB | |
| RIN ₁₂ OMA | RIN | | | -128 | dB/Hz | |
| Eye Mask Definition | | Accordi | ng to IEEE 80 | 2.3ae | | 1 |
| Optical Return Loss Tolerance | ORLT | | | 12 | dB | |
| Average Launch Power of Off Transmitter | Poff | | | -30 | dBm | |
| Receiver | | | | | | |
| Stressed Receiver Sensitivity in OMA | Psen | | | -10.3 | dBm | 2 |
| Receiver Sensitivity in OMA | Psen | | | -12.6 | dBm | 2 |
| Power Overload | Ро | 0.5 | | | dBm | |
| Signal Detect Assert Level | PSD | | | -13 | dBm | |
| Signal Detect Hysteresis | PSD | 1 | | | dB | |
| Center Wavelength Range | λ | 1260 | | 1355 | nm | |

Notes:

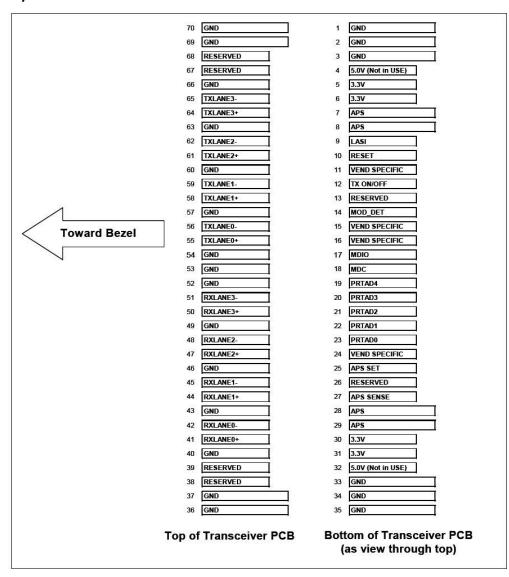
- 1. Conforms to IEEE triple trade-off between center wavelength, RMS spectral width, and minimum OMA.
- 2. Receiver sensitivity, which is defined for an ideal input signal, is informative only.

Pin Descriptions

| Item # | Signal Name | Level | I/O | Pin | Name/Description |
|--------|------------------------------------|------------|-----|---|---|
| 1 | GND | | | 1, 2, 3, 33, 34, 35, 36, 37, 40, 43, 46, 49, 52, 53, 54, 57, 60, 63, 66, 69, 70 | Ground connection for signal ground on the module. |
| 2 | APS | +1.2V | | 7, 8, 28, 29 | Input from Adaptive Power Supply. |
| 3 | APS SENSE | +1.2V | | 27 | APS Sense Output. Connected to the APS sense output. Connected to the APS input from APS. |
| 4 | APS SET | | | 25 | Feedback Input from APS. Connected to the GND through a $1.18 \mathrm{k}\Omega$ resistor inside the transponder. |
| 5 | 3.3V | +3.3 V DC | | 5, 6, 30, 31 | DC Power Input,+5.0V DC, Nominal. |
| 6 | Reserved | | | 25 | Reserved for APD. |
| 7 | Reserved | | | 13 | Reserved. |
| 8 | MDIO | Open Drain | I/O | 17 | Management Data I/O. Requires external $10\text{-}22\text{k}\Omega$ pull-up to the APS on the host. |
| 9 | MDC | 1.2V CMOS | 1 | 18 | Management Data Clock Input. |
| 10 | PRTAD4 | 1.2V CMOS | 1 | 19 | Port Address Input Bit 4. |
| 11 | PRTAD3 | 1.2V CMOS | 1 | 20 | Port Address Input Bit 3. |
| 12 | PRTAD2 | 1.2V CMOS | 1 | 21 | Port Address Input Bit 2. |
| 13 | PRTAD1 | 1.2V CMOS | 1 | 22 | Port Address Input Bit 1. |
| 14 | PRTAD0 | 1.2V CMOS | 1 | 23 | Port Address Input Bit 0. |
| 15 | LASI | Open Drain | 0 | 9 | Link Alarm Status Interrupt Output. Open drain compatible output with 10 - 20kΩ pullup on the host. Logic high = normal operation. Logic low = status flag triggered. |
| 16 | RESET | Open Drain | I | 10 | Reset Input. Open drain compatible input with $22k\Omega$ pull-up to APS internal to the transponder. Logic high = normal operation. Logic low = reset. |
| 17 | Vendor-Specific | | | 11, 15, 16, 24 | Vendor-Specific Pins. Leave unconnected when not used. |
| 18 | TX ON/OFF | Open Drain | I | 12 | TX ON/OFF Input. Open drain compatible input with $22k\Omega$ pull-up to APS internal to the transponder. Logic high = transmitter on. Logic low = transmitter off. |
| 19 | MOD DETECT | | 0 | 14 | Pulled low inside the transponder through a $1k\Omega$ resistor to the ground. |
| 20 | Reserved | | _ | 67, 68, 38, 39 | Reserved for future use. |
| 21 | TX LANE 3- TX LANE 3+ | | 1 | 65 64 | Module XAUI Input Lane 3– Module XAUI Input Lane 3+ |
| 22 | TX LANE 2- TX LANE 2+ | | ı | 62 61 | Module XAUI Input Lane 2– Module XAUI Input Lane 2+ |
| 23 | TX LANE 2+ TX LANE 1- TX LANE 1+ | | 1 | 59 58 | Module XAUI Input Lane 2+ Module XAUI Input Lane 1- Module XAUI Input Lane 1+ |

| 24 | TX LANE 0- | 1 | 56 | Module XAUI Input Lane 0– |
|----|------------|---|----|----------------------------|
| 24 | TX LANE 0+ | 1 | 55 | Module XAUI Input Lane 0+ |
| 25 | RX LANE 0+ | 0 | 41 | Module XAUI Output Lane 0+ |
| 25 | RX LANE 0- | U | 42 | Module XAUI Output Lane 0– |
| 26 | RX LANE 1+ | 0 | 44 | Module XAUI Output Lane 1+ |
| 20 | RX LANE 1- | U | 45 | Module XAUI Output Lane 1– |
| 27 | RX LANE 2+ | 0 | 47 | Module XAUI Output Lane 2+ |
| 21 | RX LANE 2- | U | 48 | Module XAUI Output Lane 2– |
| 20 | RX LANE 3+ | 0 | 50 | Module XAUI Output Lane 3+ |
| 28 | RX LANE 3- | 0 | 51 | Module XAUI Output Lane 3– |

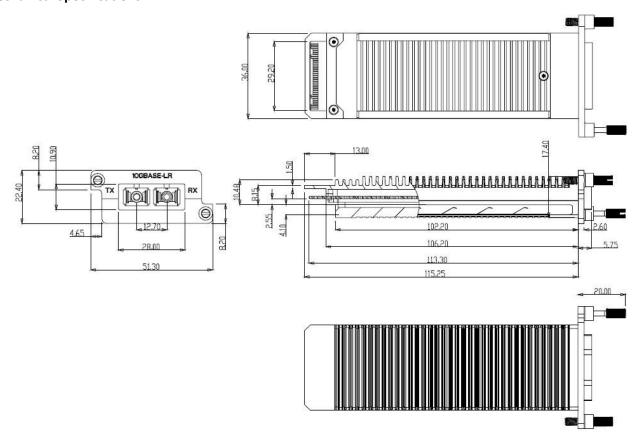
Electrical Pad Layout



Host PCB Xenpak Pin-Out

| 1 | GND | GND | 70 |
|----|-------------------|----------|----|
| 2 | GND | GND | 69 |
| 3 | GND | RESERVED | 68 |
| 4 | 5.0V (Not in USE) | RESERVED | 67 |
| 5 | 3.3V | GND | 66 |
| 6 | 3.3V | TXLANE3- | 65 |
| 7 | APS | TXLANE3+ | 64 |
| 8 | APS | GND | 63 |
| 9 | LASI | TXLANE2- | 62 |
| 10 | RESET | TXLANE2+ | 61 |
| 11 | VEND SPECIFIC | GND | 60 |
| 12 | TX ON/OFF | TXLANE1- | 59 |
| 13 | RESERVED | TXLANE1+ | 58 |
| 14 | MOD_DET | GND | 57 |
| 15 | VEND SPECIFIC | TXLANE0- | 56 |
| 16 | VEND SPECIFIC | TXLANE0+ | 55 |
| 17 | MDIO | GND | 54 |
| 18 | MDC | GND | 53 |
| 19 | PRTAD4 | GND | 52 |
| 20 | PRTAD3 | RXLANE3- | 51 |
| 21 | PRTAD2 | RXLANE3+ | 50 |
| 22 | PRTAD1 | GND | 49 |
| 23 | PRTAD0 | RXLANE2- | 48 |
| 24 | VEND SPECIFIC | RXLANE2+ | 47 |
| 25 | APS SET | GND | 46 |
| 26 | RESERVED | RXLANE1- | 45 |
| 27 | APS SENSE | RXLANE1+ | 44 |
| 28 | APS | GND | 43 |
| 29 | APS | RXLANE0- | 42 |
| 30 | 3.3V | RXLANE0+ | 41 |
| 31 | 3.3V | GND | 40 |
| 32 | 5.0V (Not in USE) | RESERVED | 39 |
| 33 | GND | RESERVED | 38 |
| 34 | GND | GND | 37 |
| 35 | GND | GND | 36 |
| | | | |

Mechanical Specifications



About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.















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