

## MCA4J80-N004-C

Mellanox® MCA4J80-N004 Compatible TAA 800GBase-CU OSFP to OSFP Direct Attach Cable (Active Twinax, 4m)  
Infiniband Only

### Features:

- Compliant to OSFP MSA Specifications
- PAM4 106.25Gbps Transmission Per Channel
- Infiniband NDR Compatible
- Low Power Consumption
- Enables Auto-Negotiation and Link Training
- 3.3V Power Supply
- Linear PAM4 Programmable Equalizer Optimized for 56GBaud Copper Link
- Low Latency: <10ps
- Operating Temperature: 0 to 70 Celsius
- RoHS Compliant and Lead-Free



### Applications:

- 800GBase Ethernet

### Product Description

This is a Mellanox® MCA4J80-N004 compatible 800GBase-CU OSFP to OSFP direct attach cable that operates over active copper with a maximum reach of 4.0m (13.1ft). It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This direct attach cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")



## General Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	Tstg	-40		85	°C
Operating Case Temperature	Tc	0		70	°C
Supply Voltage	Vcc	-0.3	3.3	3.6	V
Relative Operating Humidity	RH	5		85	%
Data Rate	DR		800		Gbps

## Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Length	L			4	M	
AWG			25		AWG	
Jacket Material		Plastic Braided Mesh Technology Net				

## Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.1	3.3	3.5		
Input Amplitude		800		1200	mVp-p	
Input Low Voltage	VIL	-0.3		0.35 x Vcc	V	
Input High Voltage	VIH	0.65 x Vcc		Vcc + 0.3	V	
Output Logic - Low	VOL			0.25 x Vcc	V	
I2C Master-Mode Output			400		kHz	
Power Consumption			1.2	1.5	W	
Raw Cable Impedance	Zca	90	100	110	$\Omega$	
Mated Connector Impedance	Zmated	85	100	115	$\Omega$	
Maximum Insertion Loss @26.56GHz	SDD21	11		19.75	dB	
Differential to Common-Mode Return Loss	SDD11/22	RLcd(f) $\geq$	$\begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.56) & 26.56 \leq f \leq 40 \end{cases}$		dB	1
Differential to Common-Mode Conversion Loss	SCD11/22	Conversion_loss(f) -	$\begin{cases} 10 & 0.05 \leq f < 12.89 \\ 14 - 0.3108f & 12.89 \leq f \leq 40 \end{cases}$		dB	1
Common-Mode to Common-Mode Return Loss	SCD21-SDD21	RLcc(f) $\geq$ 1.08			dB	1
Minimum COM	COM	3			dB	
Minimum Cable Assembly	ERL	8.25			dB	
BER				$2.4 \times 10^{-4}$		

### Notes:

1. For  $0.05 \leq f \leq 40$ GHz, where f is the frequency in GHz.

## Pin Descriptions

Pin	Symbol	Name/Description	Logic	Plug Sequence	Direction	Notes
1	GND	Module Ground.		1		
2	Tx2+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
3	Tx2-	Transmitter Data Inverted.	CML-I	3	Input from Host	
4	GND	Module Ground.		1		
5	Tx4+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
6	Tx4-	Transmitter Data Inverted.	CML-I	3	Input from Host	
7	GND	Module Ground.		1		
8	Tx6+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
9	Tx6-	Transmitter Data Inverted.	CML-I	3	Input from Host	
10	GND	Module Ground.		1		
11	Tx8+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
12	Tx8-	Transmitter Data Inverted.	CML-I	3	Input from Host	
13	GND	Module Ground.		1		
14	SCL	2-Wire Serial Interface Clock.	LVCMOS-I/O	3	Bi-Directional	1
15	Vcc	+3.3V Power.		2	Power from Host	
16	Vcc	+3.3V Power.		2	Power from Host	
17	LPWn/PRSn	Low-Power Mode/Module Present.	Multi-Level	3	Bi-Directional	2
18	GND	Module Ground.		1		
19	Rx7-	Receiver Data Inverted.	CML-O	3	Output from Host	
20	Rx7+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
21	GND	Module Ground.		1		
22	Rx5-	Receiver Data Inverted.	CML-O	3	Output from Host	
23	Rx5+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
24	GND	Module Ground.		1		
25	Rx3-	Receiver Data Inverted.	CML-O	3	Output from Host	
26	Rx3+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
27	GND	Module Ground.		1		
28	Rx1-	Receiver Data Inverted.	CML-O	3	Output from Host	
29	Rx1+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
30	GND	Module Ground.		1		
31	GND	Module Ground.		1		
32	Rx2+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
33	Rx2-	Receiver Data Inverted.	CML-O	3	Output from Host	
34	GND	Module Ground.		1		
35	Rx4+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	

<b>36</b>	Rx4-	Receiver Data Inverted.	CML-O	3	Output from Host	
<b>37</b>	GND	Module Ground.		1		
<b>38</b>	Rx6+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
<b>39</b>	Rx6-	Receiver Data Inverted.	CML-O	3	Output from Host	
<b>40</b>	GND	Module Ground.		1		
<b>41</b>	Rx8+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
<b>42</b>	Rx8-	Receiver Data Inverted.	CML-O	3	Output from Host	
<b>43</b>	GND	Module Ground.		1		
<b>44</b>	INT/RSTn	Module Interrupt/Module Reset.	Multi-Level	3	Bi-Directional	2
<b>45</b>	Vcc	+3.3V Power.		2	Power from Host	
<b>46</b>	Vcc	+3.3V Power.		2	Power from Host	
<b>47</b>	SDA	2-Wire Serial Interface Data.	LVCMOS-I/O	3	Bi-Directional	1
<b>48</b>	GND	Module Ground.		1		
<b>49</b>	Tx7-	Transmitter Data Inverted.	CML-I	3	Input from Host	
<b>50</b>	Tx7+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
<b>51</b>	GND	Module Ground.		1		
<b>52</b>	Tx5-	Transmitter Data Inverted.	CML-I	3	Input from Host	
<b>53</b>	Tx5+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
<b>54</b>	GND	Module Ground.		1		
<b>55</b>	Tx3-	Transmitter Data Inverted.	CML-I	3	Input from Host	
<b>56</b>	Tx3+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
<b>57</b>	GND	Module Ground.		1		
<b>58</b>	Tx1-	Transmitter Data Inverted.	CML-I	3	Input from Host	
<b>59</b>	Tx1+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
<b>60</b>	GND	Module Ground.		1		

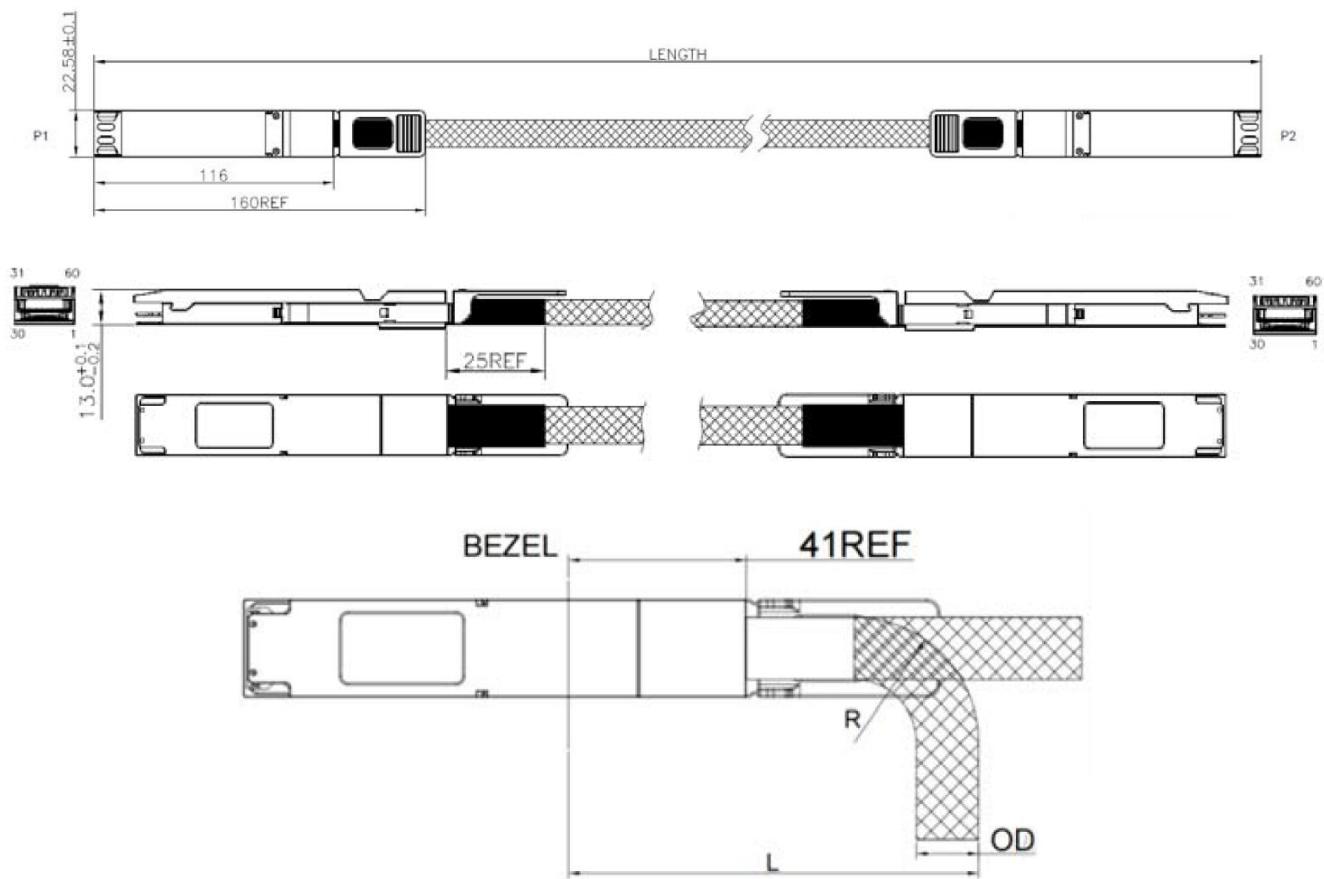
**Notes:**

1. Open-drain with pull-up resistor on the host.
2. See "Pin Assignments" below for the required circuit.

## Pin Assignments

Top Side (viewed from top)		Bottom Side (viewed from bottom)	
60	GND		
59	TX1p		
58	TX1n		
57	GND		
56	TX3p		
55	TX3n		
54	GND		
53	TX5p		
52	TX5n		
51	GND		
50	TX7p		
49	TX7n		
48	GND		
47	SDA		
46	VCC		
45	VCC		
44	INT/RSTn		
43	GND		
42	RX8n		
41	RX8p		
40	GND		
39	RX6n		
38	RX6p		
37	GND		
36	RX4n		
35	RX4p		
34	GND		
33	RX2n		
32	RX2p		
31	GND		
----- Module Card Edge -----		----- Module Card Edge -----	
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## Mechanical Specifications



### Bending Radius

Wire Gauge	OD (Ref.)	Bend Radius "R"	Min. Bend Radius "L"
25AWG	12.1mm	25mm	86mm

## About ProLabs

Our extensive experience comes as standard. For over 20 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with more than 100 optical switching and transport platforms.

## A Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 1.6T while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

## The Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure compatible products, and immediate answers to your questions. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.



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