

OSFP-2QSFP56-ADAC4M-MX-C

Mellanox® Compatible TAA 400GBase-CU OSFP to 2xQSFP56 Direct Attach Cable Direct Attach Cable (Active Twinax, 4m)

Features:

- OSFP MSA and QSFP MSA Compliant
- Infiniband HDR Compatible
- Transmission Data Rate Up to 53.125Gbps Per Channel
- Enable 400Gbps to 2x200Gbps Transmission
- Low Latency: 10ps
- Operating Temperature Range: 0 to 70 Celsius
- RoHS Compliant and Lead-Free



Applications:

- 400GBase Ethernet

Product Description

This is a Mellanox® Compatible 400GBase-CU OSFP to 2xQSFP56 direct attach cable that operates over active copper with a maximum reach of 4m. It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. We stand behind the quality of our products and proudly offer a limited lifetime warranty. This cable is TAA (Trade Agreements Act) compliant and is built to comply with MSA (Multi-Source Agreement) standards.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	-0.3	3.3	3.47	V
Storage Temperature	Tstg	-40		85	°C
Operating Case Temperature	Tc	0		70	°C
Relative Humidity	RH	5		85	%
Data Rate			400		Gbps

Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	Vcc	3.1	3.3	3.5	V
Input Amplitude		800		1200	mVp-p
Input Low Voltage	VIL	-0.3		0.35*Vcc	
Input High Voltage	VIH	0.65*Vcc		Vcc+0.3	
Output Logic Low	VOL			0.25*Vcc	
I2C Master Mode Output Frequency			400		kHz
400G End Power Consumption			1.2	1.5	W
200G End Power Consumption			0.6	0.7	W
Raw Cable Impedance	Zca	90	100	110	Ω
Mated Connector Impedance	Zmated	85	100	115	Ω
Insertion Loss @13.28GHz	SDD21	6		14	dB
Return Loss	SDD11/22	$\text{Return_loss}(f) \geq \begin{cases} 11 & 0.05 \leq f < 26.5625/7.5 \\ 6.0-9.2\lg(15f/5.5*7.5/26.5625) & 26.5625/7.5 \leq f \leq 26.5 \end{cases}$			dB
Differential to Common-Mode Return Loss	SCD11/22	$\text{Return_loss}(f) \geq \begin{cases} -25+(20/26.5625)f & 0.05 \leq f < 26.5625/2 \\ -18+(6/26.5625) & 26.5625 \leq f \leq 26.5625 \end{cases}$			dB
Differential to Common-Mode Conversion Loss	SCD21-SDD21	$\text{Conversion_loss}(f) - \text{IL}(f) \geq \begin{cases} 10 & 0.01 \leq f < 12.89 \\ 27-(29/22)f & 12.89 \leq f < 15.7 \\ 6.3 & 15.7 \leq f \leq 19 \end{cases}$			dB
Minimum COM	COM	3			dB
BER				2.4x10 ⁻⁴	

Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Length	L		4		M
Wire Gauge			30		AWG
Jacket Material		Plastic Braided Mesh, Red			

Pin Descriptions (OSFP End)

Pin	Symbol	Name/Description	Logic	Plug Sequence	Direction	Notes
1	GND	Module Ground.		1		
2	Tx2+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
3	Tx2-	Transmitter Data Inverted.	CML-I	3	Input from Host	
4	GND	Module Ground.		1		
5	Tx4+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
6	Tx4-	Transmitter Data Inverted.	CML-I	3	Input from Host	
7	GND	Module Ground.		1		
8	Tx6+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
9	Tx6-	Transmitter Data Inverted.	CML-I	3	Input from Host	
10	GND	Module Ground.		1		
11	Tx8+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
12	Tx8-	Transmitter Data Inverted.	CML-I	3	Input from Host	
13	GND	Module Ground.		1		
14	SCL	2-Wire Serial Interface Clock.	LVC MOS-I/O	3	Bi-Directional	1
15	Vcc	+3.3V Power.		2	Power from Host	
16	Vcc	+3.3V Power.		2	Power from Host	
17	LPWn/PRSn	Low-Power Mode/Module Present.	Multi-Level	3	Bi-Directional	2
18	GND	Module Ground.		1		
19	Rx7-	Receiver Data Inverted.	CML-O	3	Output to Host	
20	Rx7+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
21	GND	Module Ground.		1		
22	Rx5-	Receiver Data Inverted.	CML-O	3	Output to Host	
23	Rx5+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
24	GND	Module Ground.		1		
25	Rx3-	Receiver Data Inverted.	CML-O	3	Output to Host	
26	Rx3+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
27	GND	Module Ground.		1		
28	Rx1-	Receiver Data Inverted.	CML-O	3	Output to Host	
29	Rx1+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
30	GND	Module Ground.		1		
31	GND	Module Ground.		1		
32	Rx2+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
33	Rx2-	Receiver Data Inverted.	CML-O	3	Output to Host	
34	GND	Module Ground.		1		
35	Rx4+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	

36	Rx4-	Receiver Data Inverted.	CML-O	3	Output to Host	
37	GND	Module Ground.		1		
38	Rx6+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
39	Rx6-	Receiver Data Inverted.	CML-O	3	Output to Host	
40	GND	Module Ground.		1		
41	Rx8+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
42	Rx8-	Receiver Data Inverted.	CML-O	3	Output to Host	
43	GND	Module Ground.		1		
44	INT/RSTn	Module Interrupt/Module Reset.	Multi-Level	3	Bi-Directional	2
45	Vcc	+3.3V Power.		2	Power from Host	
46	Vcc	+3.3V Power.		2	Power from Host	
47	SDA	2-Wire Serial Interface Data.	LVC MOS-I/O	3	Bi-Directional	1
48	GND	Module Ground.		1		
49	Tx7-	Transmitter Data Inverted.	CML-I	3	Input from Host	
50	Tx7+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
51	GND	Module Ground.		1		
52	Tx5-	Transmitter Data Inverted.	CML-I	3	Input from Host	
53	Tx5+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
54	GND	Module Ground.		1		
55	Tx3-	Transmitter Data Inverted.	CML-I	3	Input from Host	
56	Tx3+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
57	GND	Module Ground.		1		
58	Tx1-	Transmitter Data Inverted.	CML-I	3	Input from Host	
59	Tx1+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
60	GND	Module Ground.		1		

Notes:

1. Open-drain with pull-up resistor on the host.
2. See pin assignments below for the required circuit.

Electrical Pin-Out Details - OSFP

Top Side (viewed from top)

60	GND	
59	TX1p	
58	TX1n	
57	GND	
56	TX3p	
55	TX3n	
54	GND	
53	TX5p	
52	TX5n	
51	GND	
50	TX7p	
49	TX7n	
48	GND	
47	SDA	
46	VCC	
45	VCC	
44	INT/RSTn	
43	GND	
42	RX8n	
41	RX8p	
40	GND	
39	RX6n	
38	RX6p	
37	GND	
36	RX4n	
35	RX4p	
34	GND	
33	RX2n	
32	RX2p	
31	GND	

Module Card Edge

Bottom Side (viewed from bottom)

	GND	1
	TX2p	2
	TX2n	3
	GND	4
	TX4p	5
	TX4n	6
	GND	7
	TX6p	8
	TX6n	9
	GND	10
	TX8p	11
	TX8n	12
	GND	13
	SCL	14
	VCC	15
	VCC	16
	LPWn/PRSn	17
	GND	18
	RX7n	19
	RX7p	20
	GND	21
	RX5n	22
	RX5p	23
	GND	24
	RX3n	25
	RX3p	26
	GND	27
	RX1n	28
	RX1p	29
	GND	30

Pin Descriptions (QSFP End)

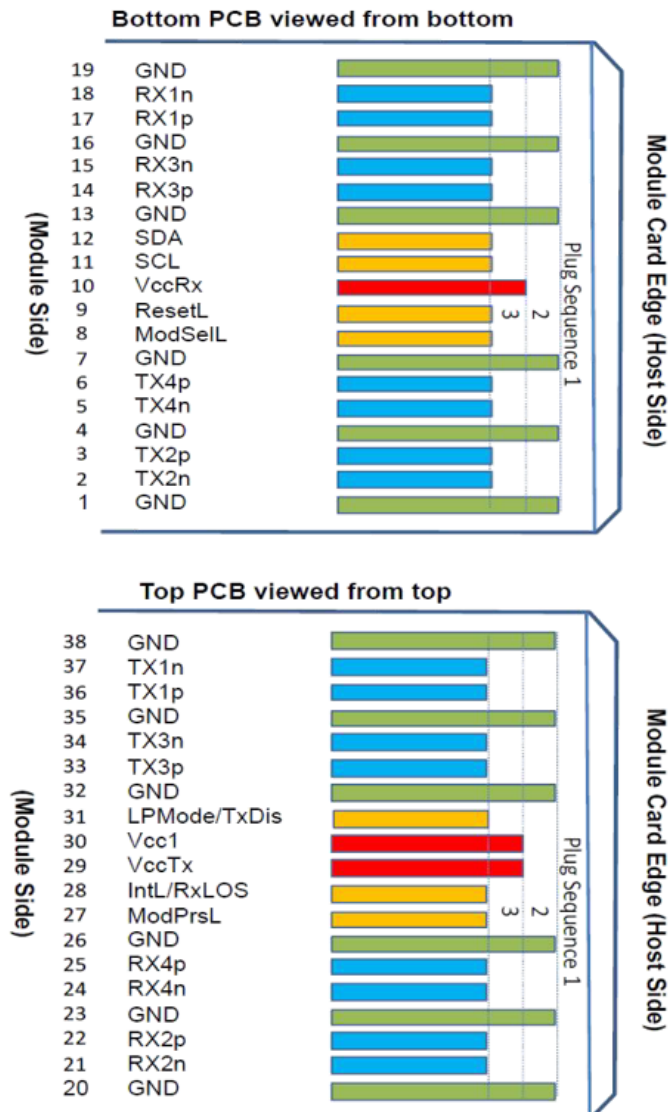
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3	
7		GND	Module Ground.	1	1
8	LVTTL-I	ModSelL	Module Select.	3	
9	LVTTL-I	ResetL	Module Reset.	3	
10		VccRx	+3.3V Receiver Power Supply.	2	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	3	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	3	
13		GND	Module Ground.	1	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3	
15	CML-O	Rx3-	Receiver Inverted Data Output.	3	
16		GND	Module Ground.	1	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3	
18	CML-O	Rx1-	Receiver Inverted Data Output.	3	
19		GND	Module Ground.	1	1
20		GND	Module Ground.	1	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	3	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3	
23		GND	Module Ground.	1	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	3	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3	
26		GND	Module Ground.	1	1
27	LVTTL-O	ModPrsL	Module Present.	3	
28	LVTTL-O	IntL	Interrupt.	3	
29		VccTx	+3.3V Transmitter Power Supply.	2	2
30		Vcc1	+3.3V Power Supply.	2	2
31	LVTTL-I	LPMODE	Low-Power Mode.	3	
32		GND	Module Ground.	1	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3	
35		GND	Module Ground.	1	1

36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3	
38		GND	Module Ground.	1	1

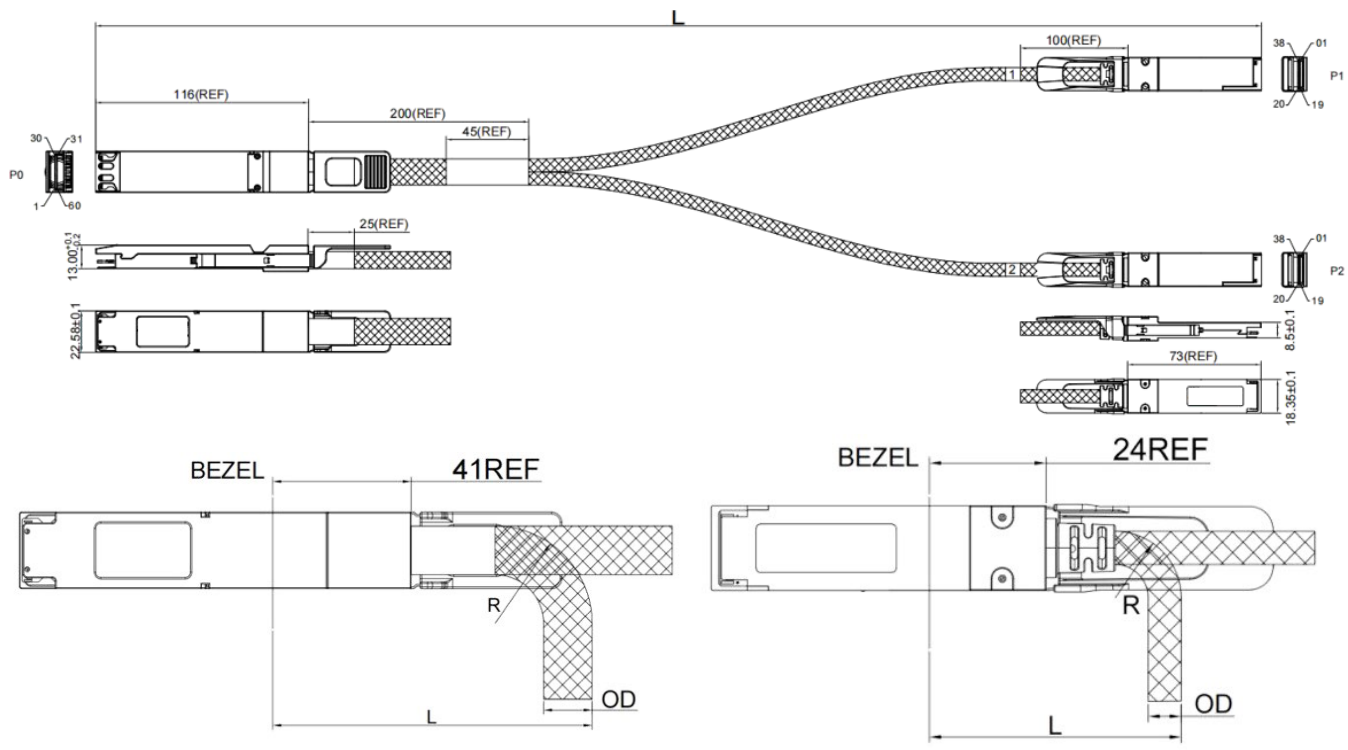
Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1, and VccTx are the receiver and transmitter power supplies and shall be applied concurrently. VccRx, Vcc1, and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Electrical Pin-Out Details - QSFP



Mechanical Specifications



OSFP				QSFP			
Gauge	OD	Bend Radius "R"	Min. Bend Radius "L"	Gauge	OD	Bend Radius "R"	Min. Bend Radius "L"
30AWG	9.5MM	18MM	60MM	30AWG	5.7MM	12MM	46MM

About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.



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