QSFP28BX89100M-C

Cisco® QSFP-40/100-SRBD Compatible 40/100GBase-SR QSFP28 Bidi Transceiver (832nm/918nm, 100m, LC, DOM)

Features:

- SFF-8665 Compliance
- Simplex LC Connector
- Single-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free

Applications:

- 40/100GBase Ethernet
- Access and Enterprise

Product Description

This Cisco® QSFP-40/100-SRBD compatible QSFP28 transceiver provides 100GBase-BX throughput up to 100m over OM4 multi-mode fiber (MMF) using a wavelength of 832nm to 918nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Cisco® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

Rev. 053023

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Ts	-40		85	˚C	
3.3V Power Supply Voltage	Vcc	-0.5		3.6	V	
Data Input Voltage – Single Ended		-0.5		Vcc + 0.5	V	
Data Input Voltage – Differential	|VDIp –- VDIn|			0.8	V	1
Control Input Voltage	Vi	-0.5		Vcc + 0.5, 3.6	V	
Control Output Current	Io	-20		20	mA	
Relative Humidity	RH	5		95	%	

Notes:

1. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry (SFF-8679). The damage threshold of the module input shall be at least 1600 mV peak-to-peak differential.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Case operating Temperature	Tc	+10		+70	˚C	1
3.3V Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Signal Rate per Channel, 100 GbE			25.78125		GBd	2
Power Supply Noise				50	mVpp	3
Receiver Differential Data Output Load			100		Ω	
Fiber Length (OM3)	0.5			70	m	4
Fiber Length (OM4)	0.5			100	m	5
Fiber Length (OM5)	0.5			150	m	6

Notes:

1. Continuous operation at the maximum recommended operating case temperature should be avoided to not degrade reliability.
2. CAUI-4 operation with no host-generated FEC. This module must not receive preceded FEC signals from the host ASIC, which will interfere with the captive FEC generated and recovered within the optical transceiver link.
3. Power supply noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Recommended Power Supply Filter figure below.
4. OM3 fiber effective modal bandwidth is 1948 MHz-km 50-µm MMF (minimum) at 847nm, 1778 MHz-km at 863 nm, 1345 MHz-km at 900 nm, and 1222 MHz-km at 916 nm per the TIA informative guidance proposal V2. The maximum link distance is based on an allocation of 1.5-dB total connection and splice loss. The loss of a single connection shall not exceed 0.75 dB.
5. OM4 fiber effective modal bandwidth is 4442 MHz-km 50-µm MMF (minimum) at 847nm, 3643 MHz-km at 863 nm, 2179 MHz-km at 900 nm, and 1878 MHz-km at 916 nm per the TIA informative guidance

proposal V2. The maximum link distance is based on an allocation of 1.5-dB total connection and splice loss. The loss of a single connection shall not exceed 0.75 dB.

6. OM5 fiber effective modal bandwidth is 4442 MHz-km 50-µm MMF (minimum) at 847 nm, 4353 MHz-km at 863 nm, 3366 MHz-km at 900 nm, and 2939 MHz-km at 916 nm per the TIA-492AAAE specification. The maximum link distance is based on an allocation of 1.5-dB total connection and splice loss. The loss of a single connection shall not exceed 0.75 dB.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Consumption				3.5	W	
Power Supply Current	ICC			1130	mA	
AC-Coupling Capacitors (Internal)			0.1		µF	

High Speed Electrical Input Characteristics

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes
Signaling Rate, Per Lane	TP1		25.78125		GBd	±100ppm
Differential Peak-to-Peak Input Voltage Tolerance	TP1a	900		1130	mV	
Differential Input Return Loss, Minimum	TP1		Eq 83E-5		dB	802.3
Differential to Common-Mode Input Return Loss (Minimum)	TP1		Eq 83E-6		dB	802.3
Differential Termination Mismatch	TP1			10	%	
Module Stressed Input Test	TP1a		83E.3.4.1			802.3
Single-ended Voltage Tolerance Range	TP1a	-0.4		3.3	V	
DC Common-Mode Output Voltage	TP1	-0.350		2.85	V	1

Notes:

1. DC common mode voltage is generated by the host. The specification includes the effects of ground offset voltage.

Parameter	Value	Units	Notes
Module Stressed Input Test			1
Eye Width	0.46	UI	
Applied Peak-to-Peak Sinusoidal Jitter	IEEE 802.3, Table 88-13		
Eye Height	95	mV	

Notes:

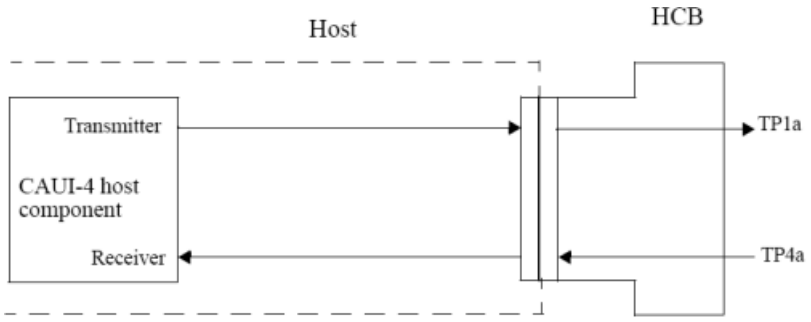
1. The module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes
Electrical Input LOS Assert Threshold, Differential Peak-to-Peak Voltage Swing	ΔVdi pp los	10			mVpp	
LOS Hysteresis		0.5		4	dB	1

Notes:

1. LOS hysteresis is defined as 20 × Log (LOS Deassert Level / LOS Assert Level)

IEEE 802.3 CAUI-4 Compliance Points TP1a, TP4a



Note:

1. A reference receiver is used to measure host eye width and eye height at TP1a. The reference receiver includes a selectable continuous time linear equalizer (CTLE), which is described by the following equation (83E-4) with coefficients given in Table 83E-2.

$$H(f) = \frac{GP_1P_2}{Z_1} \times \frac{j2\pi f + Z_1}{(j2\pi f + P_1)(j2\pi f + P_2)}$$

Where:

H(f) is the CTLE transfer function, f is the frequency in GHz
G is the CTLE gain P1, P2 are the CTLE poles in Grad/s
Z1 is the CTLE zero in Grad/s j is the square root of –1
f is the frequency in GHz

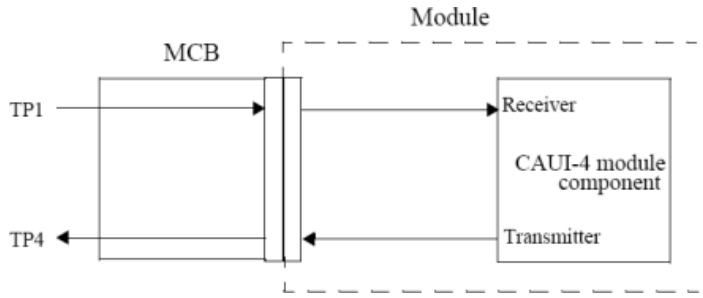
High-Speed Electrical Output Characteristics

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes
Signaling Rate, Per Lane	TP4		25.78125		GBd	±100ppm
AC Common-Mode Output Voltage (Max., RMS)	TP4			17.5	mV,rms	
Differential Output Voltage	TP4			900	mV	
Eye Width	TP4	0.57			UI	
Eye Height, Differential	TP4	228			mV	
Vertical Eye Closure	TP4			5.5	dB	
Differential Output Return Loss, Min.	TP4		Eq 83E-2		dB	802.3
Common-to-Differential Mode Conversion Return Loss (Min.)	TP4		Eq 83E-2		dB	802.3
Differential Termination Mismatch	TP4			10	%	
Transition Time (20% to 80%)	TP4	12			ps	
DC Common-Mode Voltage	TP4	-0.35		2.85	V	1

Notes:

1. Capacitively coupled module output is compatible with DC common mode voltage generated by the host. The specification includes the effects of ground offset voltage

IEEE 802.3 CAUI-4 Compliance Points TP1, TP4



High-Speed Optical Characteristics

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Rate, Per Lane			26.5625			±100ppm
Center Wavelength 1	TP2	847	855	863	nm	
Center Wavelength 2	TP2	900	908	916	nm	
RMS Spectral Width	TP2			0.60	nm	1
Average Launch Power each Lane	TP2	–6.0		+4.0	dBm	
Optical Modulation Amplitude (OMA), Each Lane	TP2	–4.0		+3.0	dBm	
OMA – TDECQ, Each Lane	TP2	–5.9			dBm	
Peak Power, Each Lane	TP2			+7.0	dBm	
TDECQ, Each Lane	TP2			4.9	dB	
Extinction Ratio, Each Lane	TP2	3.0			dB	
Optical Return Loss Tolerance	TP2			12	dB	
Encircled Flux	TP2		≥ 86% at 19 µm, ≤ 30% at 4.5 µm			2
Average Launch Power of OFF Transmitter, Each Lane	TP2			-30	dBm	
Receiver						
Signaling Rate, Per Lane			26.5625			±100ppm
Center Wavelength 1	TP3	847	855	863	nm	
Center Wavelength 2	TP3	900	908	916	nm	
Damage Threshold	TP3	+7.5			dBm	3
Receiver Reflectance	TP3			-15	dB	
Peak Input Power, Each Lane	TP3			+7.0	dBm	
Optical Modulation Amplitude (OMA), Each Lane	TP3	-5.9		+3.0	dBm	
Average Receive Power, Each Lane	TP3	-7.9		+4.0	dBm	4
Stressed Receiver Sensitivity in OMA, Each Lane	TP3			-3.0	dBm	5
Conditions of Stressed Receiver Sensitivity	TP3					6
Stressed Eye Closure (SECQ)	TP3			4.9	dB	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. If measured into type A1a.2, 50-µm fiber in accordance with IEC 61280-1-4.
3. The receiver should be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

4. Average receive power, each lane (minimum) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Measured with conformance test signal at TP3.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes
LOS Assert – OMA	TP3	-30			dBm	
LOS De-Assert – OMA	TP3			-5.9	dBm	
LOS Hysteresis	TP3	0.5			dB	

Pin Descriptions

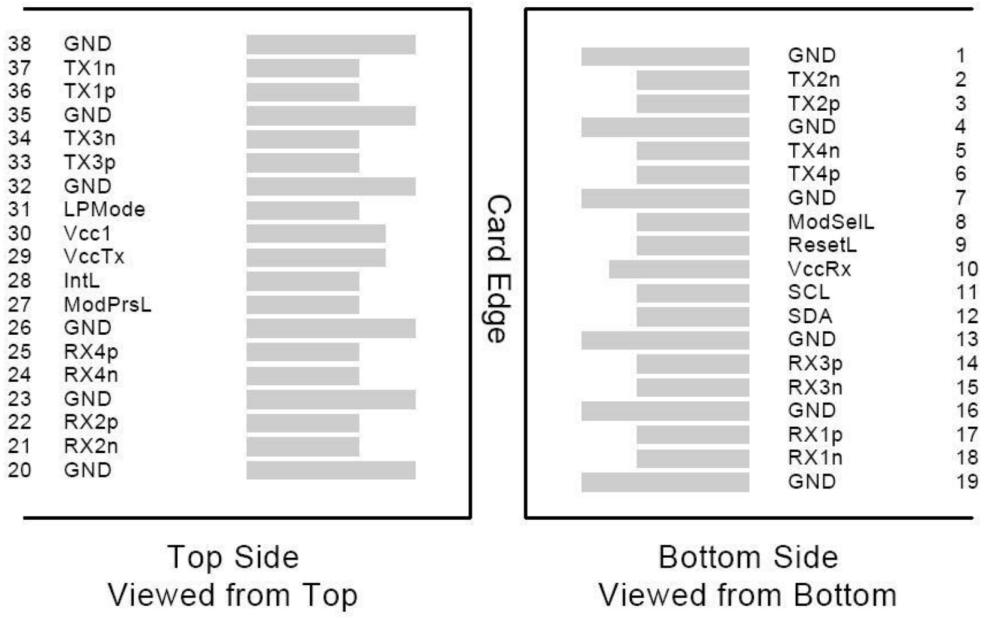
Pin	Logic	Symbol	Name/Descriptions	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	

26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

Electrical Pin-out Details



ModSeIL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

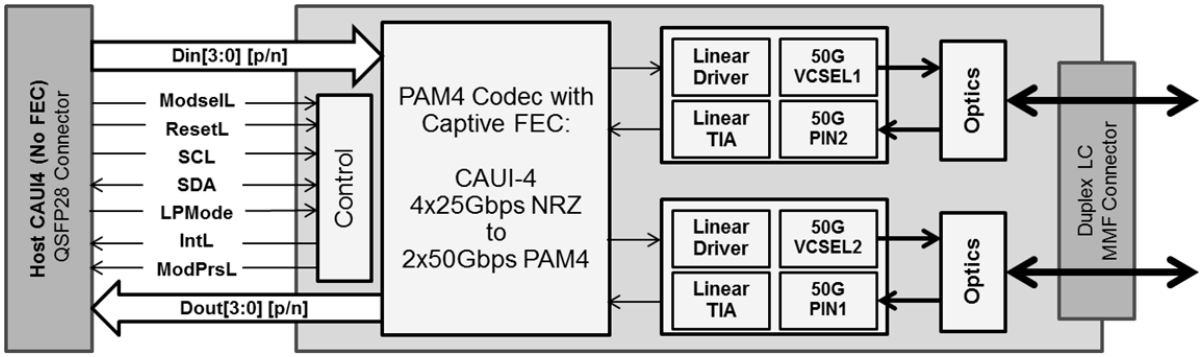
ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and de-asserted “High” when the module is physically absent from the host connector.

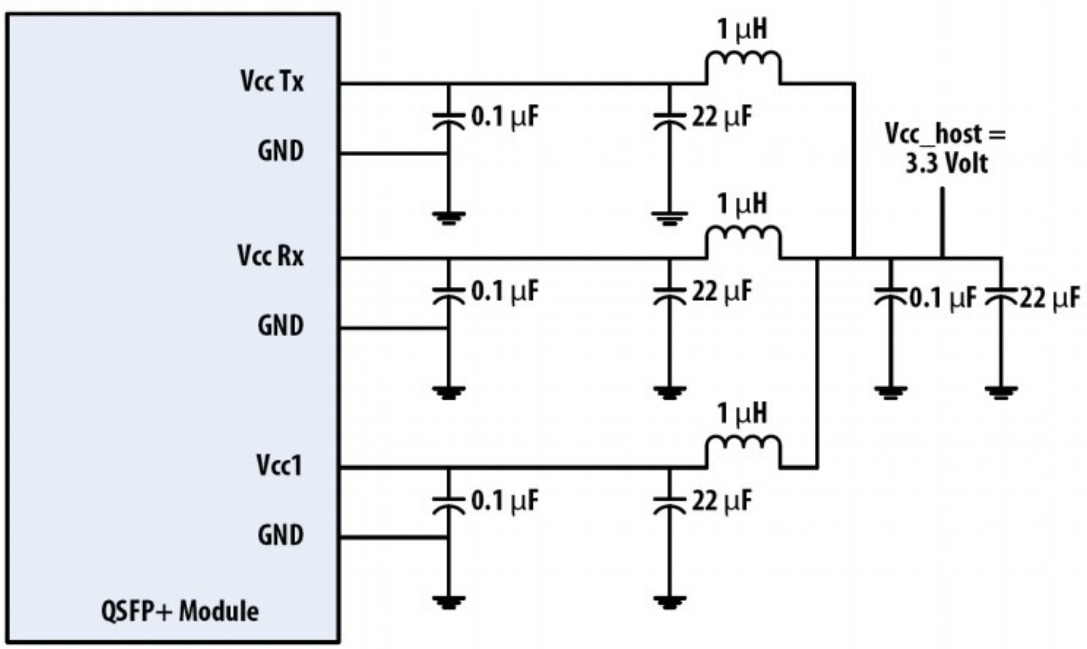
IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

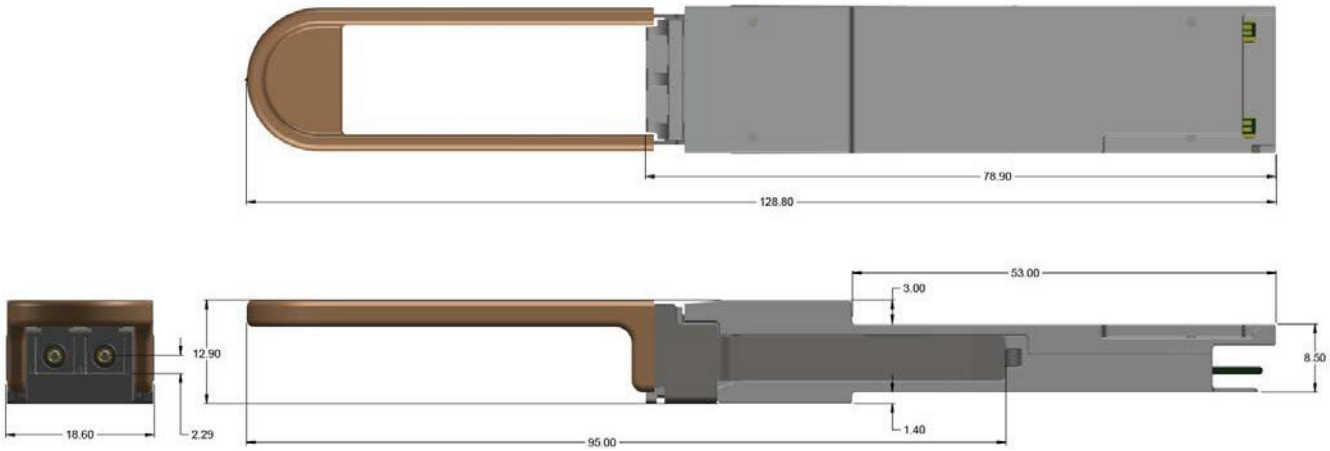
Transceiver Block Diagram



Recommended Power Supply Filter



Mechanical Specifications



About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.

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