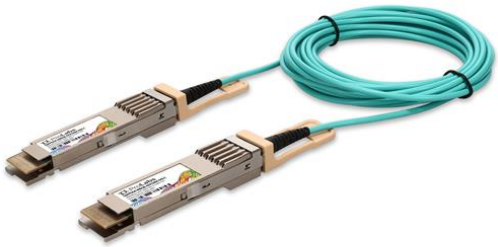
QSFPDD4-400GB-AOC50M-MX-C

Mellanox® Compatible TAA 400GBase-AOC QSFP-DD to QSFP-DD Active Optical Cable (850nm, MMF, 50m)

Features:

- Compliant to QSFP-DD MSA Standards
- 8 Parallel Full-Duplex Channels
- Compliant to IEEE802.3bs
- Up to 100m OM3 MMF Transmission
- Operating Temperature: 0 to 70 Celsius
- CMIS 4.0
- 8x53.125Gbps Electrical Interface (400GAUI-8)
- Data Rate 53.125Gbps (PAM4) Per Channel
- Maximum Power Consumption: 10.5W
- RoHS Compliant and Lead-Free



Applications:

- 400GBase Ethernet

Product Description

This is a Mellanox® Compatible 400GBase-AOC QSFP-DD to QSFP-DD active optical cable that operates over active fiber with a maximum reach of 50m. It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. We stand behind the quality of our products and proudly offer a limited lifetime warranty. This cable is TAA (Trade Agreements Act) compliant and is built to comply with MSA (Multi-Source Agreement) standards.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

Rev. 031125

General Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Supply Voltage	Vcc	-0.5		3.6	V	
Relative Operating Humidity	RH	0		85	%	
Data Rate Per Lane			26.5625			PAM4
Data Rate Accuracy		-100		100	ppm	
Link Distance with OM3	D	0.5		100	M	1

Notes:

1. FEC is required on the host system to support the maximum distance.

Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Pre-FEC Bit Error Ratio				2.4×10^{-4}		
Post-FEC Bit Error Ratio				1×10^{-12}		1
Power Consumption				10.5	W	
Supply Current	Icc			3.18	A	
Transmitter						
Signaling Rate Per Lane	TP1	26.5625 ± 100ppm			GBd	
Differential Pk-Pk Input Voltage Tolerance	TP1a	900			mVp-p	2
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common-Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				3
Single-Ended Voltage Tolerance Range (Minimum)	TP1a	-0.4 to 3.3			V	
DC Common-Mode Input Voltage	TP1	-350		2850	mV	4
Receiver						
Signaling Rate Per Lane	TP4	26.5625 ± 100ppm			GBd	
Differential Pk-Pk Output Voltage	TP4			900	mVp-p	
AC Common-Mode Output Voltage (RMS)	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common- to Differential-Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time (20-80%)	TP4	9.5			ps	
Near-End Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-End Eye Height (Differential)	TP4	70			mV	
Far-End Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-End Eye Height (Differential)	TP4	30			mV	
Far-End Pre-Cursor ISI Ratio	TP4	-4.5		2.5	%	
Common-Mode Output Voltage (Vcm)	TP4	-350		2850	mV	4

Notes:

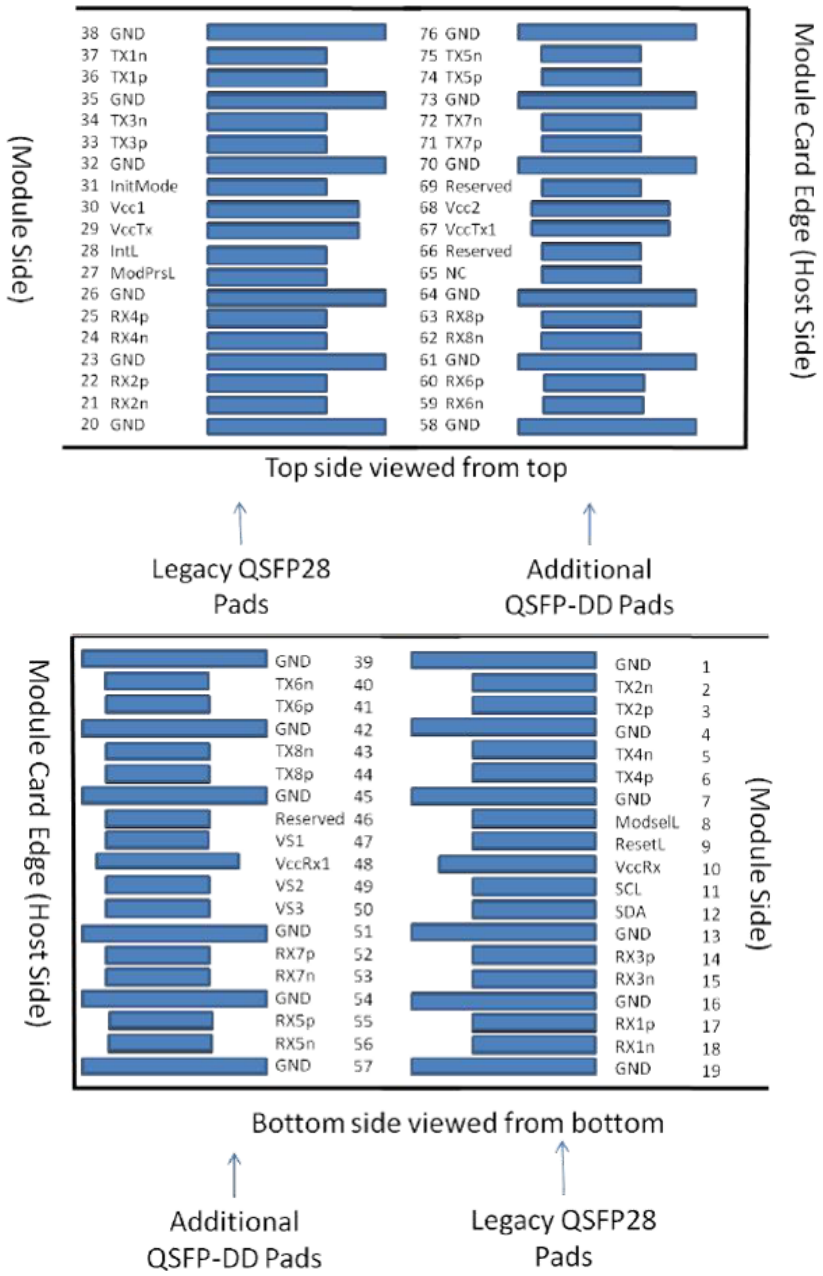
1. FEC is provided by the host system.
2. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets BER specified in IEEE 802.3bs 120E.1.1.
4. DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.

Pin Descriptions

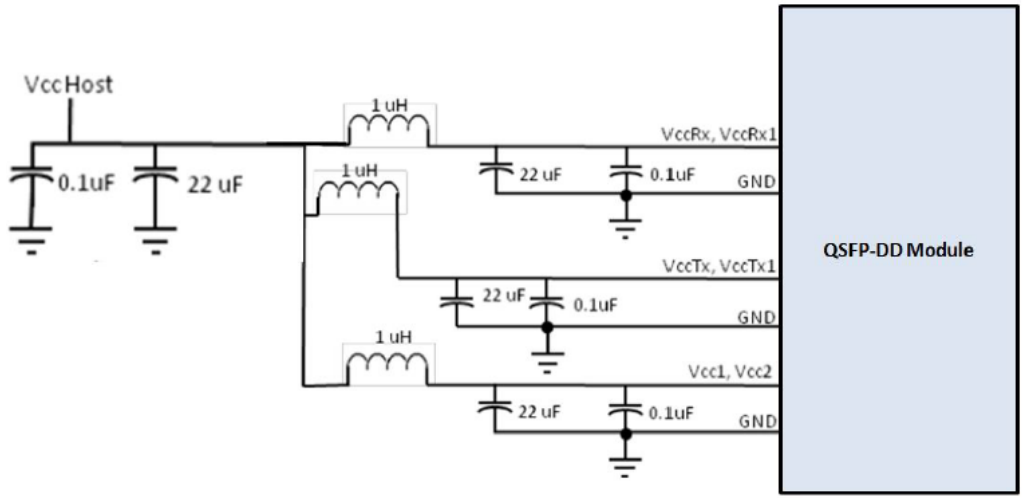
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1B	
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3B	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3B	
4		GND	Module Ground.	1B	
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3B	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3B	
7		GND	Module Ground.	1B	
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Receiver Power Supply.	2B	
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3B	
13		GND	Module Ground.	1B	
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3B	
15	CML-O	Rx3-	Receiver Inverted Data Output.	3B	
16		GND	Module Ground.	1B	
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3B	
18	CML-O	Rx1-	Receiver Inverted Data Output.	3B	
19		GND	Module Ground.	1B	
20		GND	Module Ground.	1B	
21	CML-O	Rx2-	Receiver Inverted Data Output.	3B	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3B	
23		GND	Module Ground.	1B	
24	CML-O	Rx4-	Receiver Inverted Data Output.	3B	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3B	
26		GND	Module Ground.	1B	
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL	Interrupt.	3B	
29		VccTx	+3.3V Transmitter Power Supply.	2B	
30		Vcc1	+3.3V Power Supply.	2B	
31	LVTTL-I	InitMode	Initialization Mode. In legacy QSFP applications, the InitMode pad is called LPMODE.	3B	
32		GND	Module Ground.	1B	
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3B	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3B	
35		GND	Module Ground.	1B	
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3B	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3B	
38		GND	Module Ground.	1B	
39		GND	Module Ground.	1A	
40	CML-I	Tx6-	Transmitter Inverted Data Input.	3A	

41	CML-I	Tx6+	Transmitter Non-Inverted Data Input.	3A	
42		GND	Module Ground.	1A	
43	CML-I	Tx8-	Transmitter Inverted Data Input.	3A	
44	CML-I	Tx8+	Transmitter Non-Inverted Data Input.	3A	
45		GND	Module Ground.	1A	
46		Reserved	For Future Use.	3A	
47		VS1	Module Vendor-Specific 1.	3A	
48		VccRx1	+3.3V Receiver Power Supply.	2A	
49		VS2	Module Vendor-Specific 2.	3A	
50		VS3	Module Vendor-Specific 3.	3A	
51		GND	Module Ground.	1A	
52	CML-O	Rx7+	Receiver Non-Inverted Data Output.	3A	
53	CML-O	Rx7-	Receiver Inverted Data Output.	3A	
54		GND	Module Ground.	1A	
55	CML-O	Rx5+	Receiver Non-Inverted Data Output.	3A	
56	CML-O	Rx5-	Receiver Inverted Data Output.	3A	
57		GND	Module Ground.	1A	
58		GND	Module Ground.	1A	
59	CML-O	Rx6-	Receiver Inverted Data Output.	3A	
60	CML-O	Rx6+	Receiver Non-Inverted Data Output.	3A	
61		GND	Module Ground.	1A	
62	CML-O	Rx8-	Receiver Inverted Data Output.	3A	
63	CML-O	Rx8+	Receiver Non-Inverted Data Output.	3A	
64		GND	Module Ground.	1A	
65		NC	Not Connected.	3A	
66		Reserved	For Future Use.	3A	
67		VccTx1	+3.3V Transmitter Power Supply.	2A	
68		Vcc2	+3.3V Power Supply.	2A	
69		Reserved	For Future Use.	3A	
70		GND	Module Ground.	1A	
71	CML-I	Tx7+	Transmitter Non-Inverted Data Input.	3A	
72	CML-I	Tx7-	Transmitter Inverted Data Input.	3A	
73		GND	Module Ground.	1A	
74	CML-I	Tx5+	Transmitter Non-Inverted Data Input.	3A	
75	CML-I	Tx5-	Transmitter Inverted Data Input.	3A	
76		GND	Module Ground.	1A	

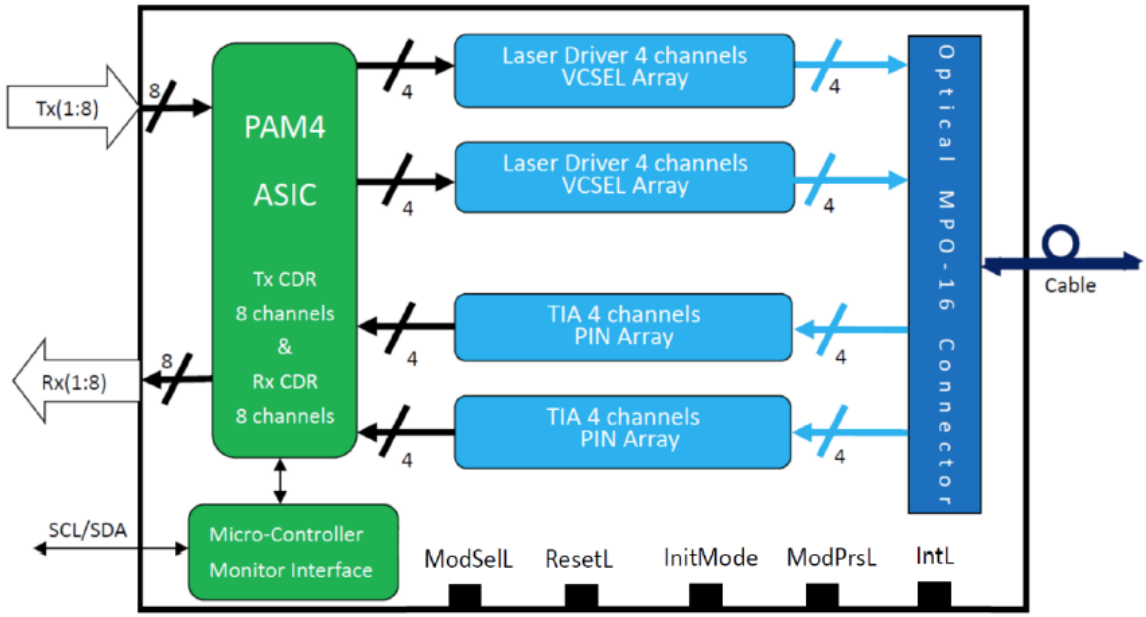
Electrical Pin-Out Details



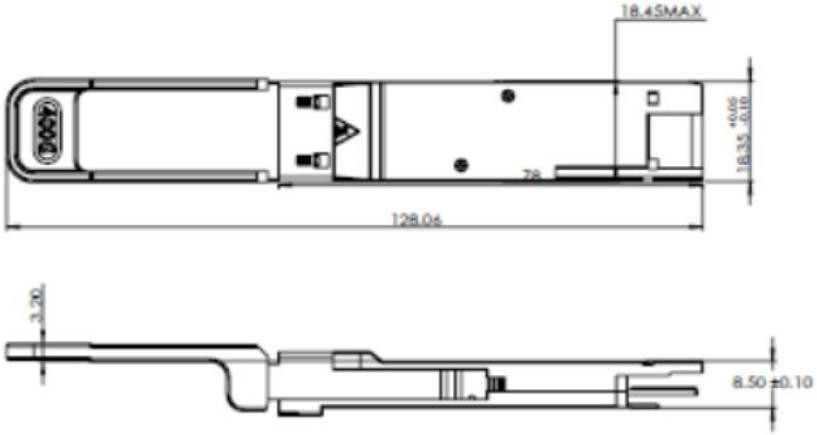
Recommended Power Supply Filter



Block Diagram



Mechanical Specifications



About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.

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