CFP MSA
CFP4 Hardware Specification

Revision 1.1
18 Mar 2015

Description:

This CFP Multi-Source Agreement (MSA) defines the CFP4 form factor of an optical transceiver to support 40Gbit/s and 100Gbit/s interfaces for Ethernet, Telecommunication and other applications. The members of the CFP MSA have authored this document to provide an industry standard form factor for new and emerging high speed communications interfaces. Specifications provided in this document are given as a “delta” to the CFP MSA Hardware Specification Rev.1.4, June 7, 2010 or the CFP MSA CFP2 Hardware Specification Rev. 1.0, July 31, 2013.

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REVISION HISTORY

Draft	Date	Revised Items
0.1	3/2/2014	Initial draft, based on CFP4 Baseline Design, Revision P
0.2	6/28/2014	2nd draft, based on revised CFP4 Baseline Design, Revision R. Some editorial errors were corrected in Rev.R Added description on Pin-out definition.
1.0	8/28/2014	First Official Release, based on CFP4 Baseline Design, Revision R
1.1	3/18/2015	Reference Document, reflecting MIS latest version Table.1-1, corrected note.1 as per MIS definition on Programmable Control 1

TABLE LIST

FIGURE LIST

REFERENCE DOCUMENTS

[1] CFP MSA Hardware Specification, Revision 1.4, June 7, 2010.

[2] CFP MSA CFP2 Hardware Specification, Revision 1.0, July 31, 2013.

[3] CFP MSA Management Interface Specification, Version 2.4, March, 2015.

[4] IEEE P802.3bm, 40Gbit/s and 100Gbit/s Operation Over Fiber Optic Cables Task Force, http://www.ieee802.org/3/bm/index.html

[5] IEEE Std 802.3™-2012, *Annexes 83A, 83B, and 86A.*

[6] IEEE Std 802.3™-2012, Cl. 45, Management Data Input/Output (MDIO) Interface.

[7] ITU-T Recommendation G.709 (2012) *Interfaces for the Optical Transport Network (OTN).*

[8] ITU-T Recommendation G.707 (2007) *Network node interface for the synchronous digital hierarchy (SDH).*

[9] OIF-CEI-3.0, http://www.oiforum.com/public/documents/OIF_CEI_03.0.pdf

[10] SFF Committee INF-8077i 10 Gigabit Small Form Factor Pluggable Module

[11] SFF Committee SFF-8431 Specifications for Enhanced Small Form Factor Pluggable Module SFP+

1 GENERAL

1.1 SCOPE

This CFP Multi-Source Agreement (MSA) defines the CFP4 form factor of an optical transceiver which can support 40Gbit/s and 100Gbit/s interfaces for Ethernet, ITU-T OTN and other applications. Specifications provided in this document are given as a "delta" to the CFP MSA Hardware Specification Rev.1.4 or the CFP2 Hardware Specification Rev. 1.0.

The CFP4 electrical interface will vary by application, but the nominal signaling lane rate is 25Gbit/s per lane and documentation is provided in OIF CEI-28G-VSR, CAUI-4, and OTL4.4 electrical interface specifications. The CFP4 electrical interface can also optionally support a nominal signaling lane rate of 10Gbit/s and documentation is provided in XLAUI, XLPPI, OTL3.4 and STL256.4. The CFP4 module may be used to support single mode and multimode fiber optics.

The CFP4 modules and the host system are hot-pluggable. The module or the host system shall not be damaged by insertion or removal of the module.

CFP MSA is an acronym for 100G[1] Form factor Pluggable Multi-Source Agreement.

1.2 CFP4 FUNCTIONAL BLOCK DIAGRAM

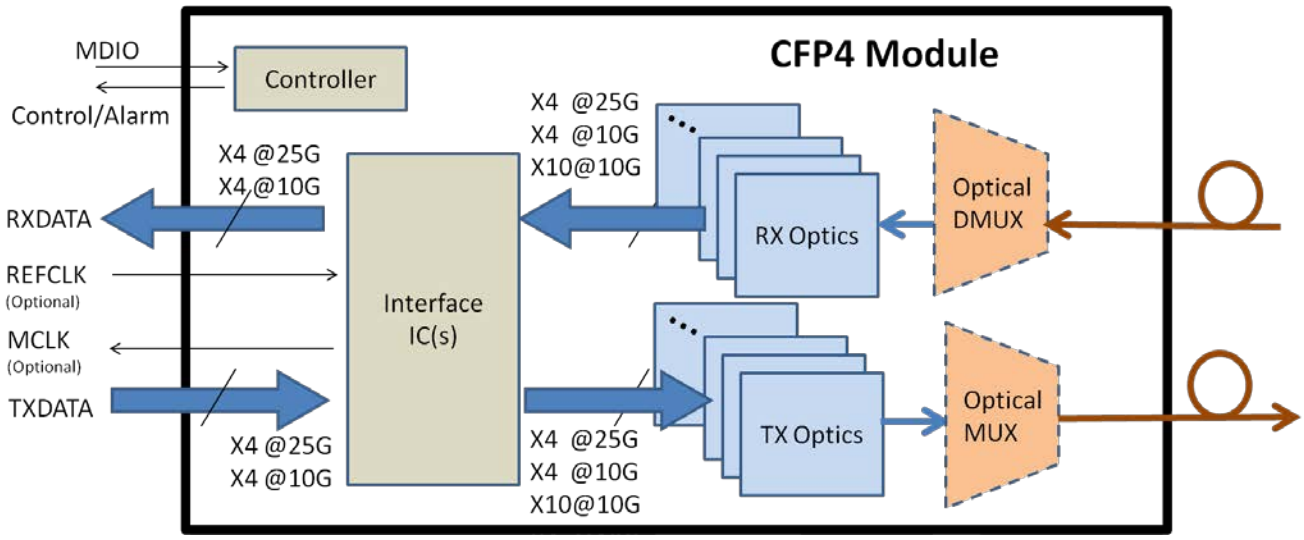


Figure 1-1: CFP4 Functional Block Diagram

1.3 FUNCTIONAL DESCRIPTION

[1] C = 100 in Roman numerals; Centum

The CFP4 module is a hot pluggable form factor designed for optical networking applications. The module size has been chosen to accommodate a wide range of power dissipations and applications. The module electrical interface has been generically specified to allow for supplier-specific customization around various “4 x 25Gbit/s” and 4 x 10Gbit/s interfaces.

1.3.1 Hot Pluggable

A CFP4 module is defined to be hot pluggable. Hot Pluggable is defined as permitting module plugging and unplugging with Vcc applied, with no module damage and predictable module behavior as per the State Transition Diagram. As shown in Figure 5-6: Pin Map Connector Engagement, the Module Absent (MOD_ABS) pin and Module Low Power (MOD_LOPWR) pin are physically guaranteed to be one of the last pins to mate.

2 CFP4 HARDWARE SIGNALING PINS

The control and status reporting functions between a host and a CFP4 module use non-data control and status reporting pins on the 56-pin connector. The control and status reporting pins work together with the MDIO interface to form a complete HOST-CFP4 management interface. The status reporting pins provide status reporting. There are three (3) Hardware Control pins, two (2) Hardware Alarm pins, and six (6) pins dedicated to the MDIO interface. Specification of the CFP4 hardware signaling pins are given in Ref.[1] with the following changes listed in this document.

2.1 Hardware Control Pins

The CFP4 Module supports real-time control functions via hardware pins, listed in
Table 1-1. Specifications of the CFP4 hardware control pins are given in Ref.[1], with the following changes listed below.

Table 1-1: Control Pins

Pin #	Symbol	Description	I/O	Logic	“H”	“L”	Pull-up /down
11	TX_DIS (PRG_CNTL)	Transmitter Disable (Optionally configurable as Programmable Control after Reset[1])	I	3.3V LVCMOS	Disable[2]	Enable[2]	Pull – Up[3]
14	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull – Up[3]
16	MOD_RSTn	Module Reset, Active Low (invert)	I	3.3V LVCMOS	Enable	Reset	Pull – Down[4]

[1] When Programmable Control is configured, MSA Default is TXDIS.

[2] Per CFP MSA Management Interface Specification [3] when PRG_CNTL is configured for this pin.

[3] Pull-Up resistor (4.7 kOhm to 10 kOhm) is located within the CFP4 module

[4] Pull-Down resistor (4.7 kOhm to 10 kOhm) is located within the CFP4 module

2.2 Hardware Control Pins: Functional Description

2.2.1 Programmable Control (PRG_CNTL)

This control pin allows for the system to program certain controls via a Hardware pin. TX Disable Pin (TX_DIS) is optionally configurable as Programmable Control 1 Pin after Reset. When Programmable Control 1 is configured,

the default setting for Control 1 is control of the TX_DIS.

2.2.1.1 Programmable Control 1 Pin

Programmable Control 1 Pin is an input pin from the Host, operating with programmable logic. This pin is pulled up in the CFP4 module. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. The CFP MSA specifies that the default function be TX Disable (TX_DIS) with active-high logic. If the other function besides TX_DIS is configured for this pin, there is no way to assert TX disable via a hardware pin.

2.2.1.2 Programmable Control 2 Pin

Not supported in CFP4 module

2.2.1.3 Programmable Control 3 Pin

Not supported in CFP4 module

2.2.1.4 Hardware Interlock

Not supported in CFP4 module

2.2.2 TX Disable Pin

TX Disable Pin (TX_DIS) is an input pin from the Host, operating with active-high logic. This pin is pulled up in the CFP4. When TX_DIS is asserted, all of the optical outputs inside a CFP4 module shall be turned off. When this pin is de-asserted, transmitters in a CFP4 module shall be turned on according to a predefined TX turned-on process which is defined by the state diagram shown in the “CFP MSA Management Interface Specification”. A maximum time is defined for the transmitter turn-on process. This time is vendor and/or technology specific and the value is stored in a MDIO register.

This pin can be optionally configured as Programmable Control 1 Pin after Reset. One MDIO register which defines if the module supports this optional configuration or not is prepared in NVR region.

Please refer to Ref.[3] for more details.

2.3 Hardware Alarm Pins

The CFP4 Module supports alarm hardware pins as listed in Table 1-2. Specifications of the CFP4 hardware alarm pins are given in Ref.[1].

Table 1-2: Hardware Alarm Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
12	RX_LOS (PRG_ALRM)	Receiver Loss of Signal (Optionally configurable as Programmable Alarm after Reset[1])	O	3.3V LVCMOS	Loss of Signal[2]	OK[2]	
15	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull Down[3]

[1] When Programmable Alarm is configured, MSA Default is HIPWR_ON.
[2] Active High per CFP MSA MIS Ref. [3] when PRG_ALRM is configured for this pin.
[3] Pull-Down resistor (<100Ohm) is located within the CFP4 module. Pull-up should be located on the host.

2.4 Hardware Alarm Pins: Functional Description

2.4.1 Programmable Alarm (PRG_ALRM)

This alarm pin allows for the system to program module supported alarms to Hardware pin. The intention is to allow for maximum design and debug flexibility.

2.4.1.1 Programmable Alarm 1 Pin

Programmable Alarm 1 Pin (PRG_ALRM1) is an output pin to the Host, operating with programmable logic. This pin can be re-programmed over MDIO registers to another MDIO alarm register while the module is in any steady state except Reset. CFP-MSA specifies the default function to be Receiver Loss of Signal (RX_LOS) indicator with active-high logic.

2.4.1.2 Programmable Alarm 2 Pin

Not supported in CFP4 module

2.4.1.3 Programmable Alarm 3 Pin

Not supported in CFP4 module

2.4.3 Receiver Loss of Signal Pin

The Receiver Loss of Signal Pin (RX_LOS) is an output pin to the Host, operating with active-high logic. When asserted, it indicates received optical power in the CFP4 module is lower than the expected value. The optical power at which RX_LOS is asserted may be specified by other governing documents and the CFP4 module vendor as the alarm threshold level is application specific. The RX_LOS is the logic OR of the LOS signals from all the input receiving channels in a CFP4 module.

This pin can be optionally configured as Programmable Alarm 1 Pin after Reset. One MDIO register which defines if the module supports this optional configuration or not is prepared in NVR region.

Please refer to Ref.[3] for more details.

2.5 Management Interface Pins

The CFP4 Module supports alarm, control and monitor functions via an MDIO bus. Upon module initialization, these functions are available. CFP4 MDIO electrical interface consists of 6pins including 2pins for MDC and MDIO, 3 Physical Port Address pins and th Global Alarm pin. MDC is the MDIO Clock line driven by the host and MDIO is the bidirectional data line driven by both the host and module depending upon the data directions. The CFP4 MDIO pins are listed in Table 1-3. Specifications of the CFP4 hardware management interface pins are given in Ref.[2] with the following changes listed below.

Table 1-3: Management Interface Pins (MDIO)

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
13	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm	
17	MDC	MDIO Clock	I	1.2V LVCMOS			
18	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
19	PRTADR0	MDIO Physical Port address bit 0	I	1.2V LVCMOS	per CFP MSA MIS Ref. [3]		
20	PRTADR1	MDIO Physical Port address bit 1	I	1.2V LVCMOS			
21	PRTADR2	MDIO Physical Port address bit 2	I	1.2V LVCMOS			

2.6 CFP4 Management Interface Hardware Description

Per specifications given in Ref.[2] .

2.7 Hardware Signaling Pin Electrical Specifications

2.7.1 Control & Alarm Pins: 3.3V LVCMOS Electrical Characteristics

The hardware control and alarm pins specified as 3.3V LVCMOS functionally described above shall meet the characteristics described in Ref.[1]. Reference figures are provided regarding pin termination; see Figure 2-1 and 2-2.

Figure 2-1: Reference +3.3V LVCMOS Output Termination

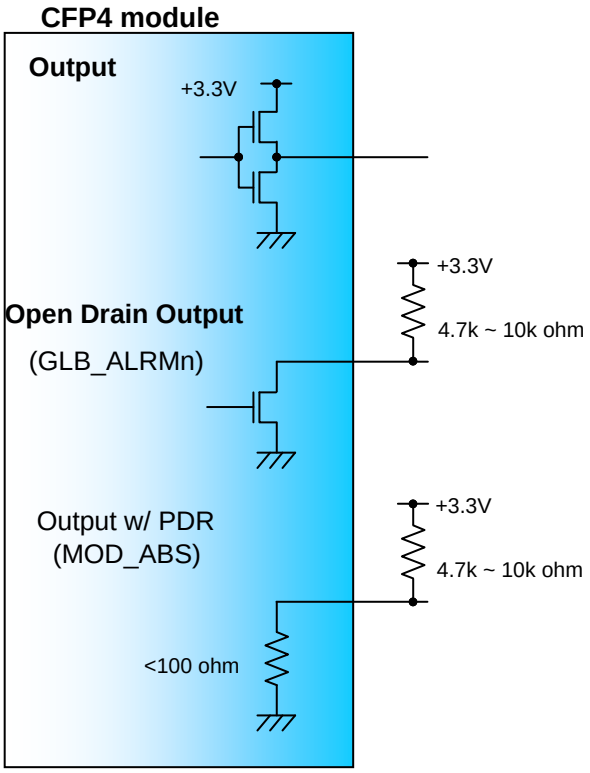
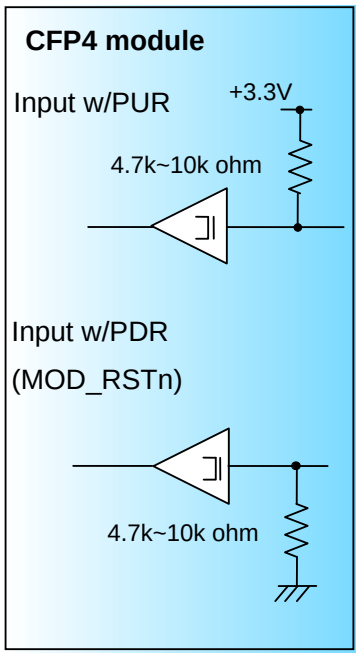


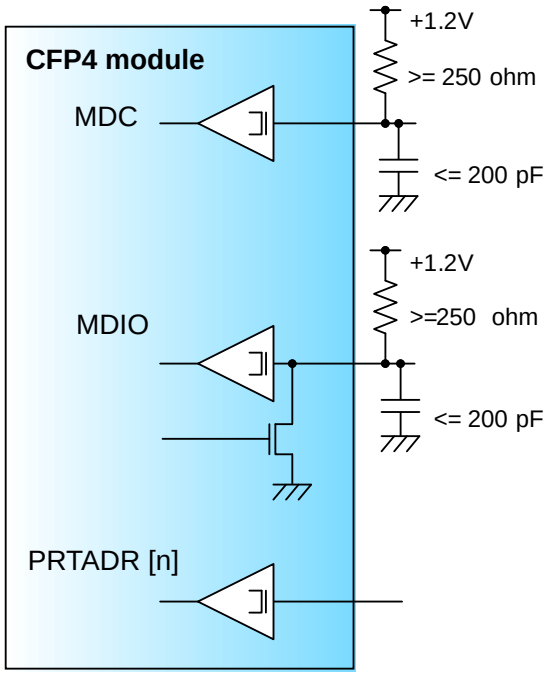
Figure 2-2: Reference 3.3V LVCMOS Input Termination



2.7.2 MDIO Interface Pins: 1.2V LVCMOS Electrical Characteristics

The MDIO interface pins specified as 1.2V LVCMOS functionally described above shall meet the characteristics described in Ref.[1]. Reference figure is provided regarding pin termination; see Fig.2-3.

Figure 2-3: Reference MDIO Interface Termination[2]



2.8 Hardware Signaling Pin Timing Requirements

Per specifications given in Ref.[2]

3 MODULE MANAGEMENT INTERFACE DESCRIPTION

[2] The MSA recommends host termination resistor value of 560 Ohms, which provides the best balance of performance for both open-drain and active tri-state driver in the module. Host termination resistor values below 560Ohms are allowed, to a minimum of 250 Ohms, but this degrades active driver performance. Host termination resistor values above 560 Ohms are allowed but this degrades open-drain driver performance.

The above drawings, with maximum host load capacitance of 200pF, also define the measurement set-up for module MDC timing verification. The capacitor in the drawing indicates the stray capacitance on the line. Don't put any physical capacitor on the line.

The CFP4 module utilizes MDIO IEEE Std 802.3™-2012 clause 45 [8] for its management interface. The CFP4 MDIO implementation is defined in a separate document entitled, “CFP MSA Management Interface Specification” [3]. When multiple CFP4 modules are connected via a single bus, a particular CFP4 module can be selected by using the Physical Port Address pins.

4 PERFORMANCE SPECIFICATIONS

4.1 OPERATING ENVIRONMENT

Per specifications given in Ref. [1]

4.2 POWER SUPPLIES AND POWER DISSIPATION

4.2.1 Voltage power supply and power dissipation

The CFP4 module power supply and maximum power dissipation specifications are defined in Table 4-1.

4.2.2 Inrush current

The inrush current on the 3.3V power supply shall be limited by the CFP4 module to assure a maximum rate of change defined in Table 4-1.

4.2.3 Turn-off current

The CFP4 module shall limit the turn-off current to assure a maximum rate of change per Table 4-1.

4.2.4 Power Supply Noise Susceptibility

A host system will supply stable power to the module and guarantee that noise & ripple on the power supply does not exceed that defined in Table 4-1. A possible example of a power supply filtering circuit that might be used on the host system is a PI C-L-C filter. A module will meet all electrical requirements and remain fully operational in the presence of noise on the 3.3V power supply which is less than that defined in the table 4-1. The component values of power supply noise filtering circuit, such as the capacitor and inductor, must be selected such that maximum Inrush and Turn-off current does not cause voltage transients which exceed the absolute maximum power supply voltage, all specified in Table 4-1.

Table 4-1: Voltage Power Supply

Parameters		Symbol	Min	Typ.	Max	Unit
Absolute Maximum Power Supply Voltage		VCC	-	-	3.6	V
Total Power Dissipation	Class 1	Pw	-	-	1.5	W
	Class 2		-	-	3	
	Class 3		-	-	4.5	
	Class 4		-	-	6	
	Class 5		-	-	7.5	
	Class 6		-	-	9	
Low Power Mode Dissipation		Plow	-	-	1	W
Operating Power Supply Voltage		VCC	3.2	3.3	3.4	V
Operating Power Supply Current[1]	Class 1 and 2	ICC	-	-	0.93	A
	Class 3 and 4		-	-	1.87	
	Class 5 and 6		-	-	2.81	
Inrush Current[2]	Class 1, 2, 3 and 4	I-inrush	-	-	100	mA/usec
Turn-off Current		I-turnoff	-100	-	-	
Inrush Current[2]	Class 5 and 6	I-inrush	-	-	200	
Turn-off Current		I-turnoff	-200	-	-	
Power Supply Noise		Vrip	-	-	2% 3%	DC – 1MHz 1 – 10MHz

[1] Maximum current per pin shall not exceed 500mA. Those power classes for which the maximum current per pin exceeds 500mA will require agreement from an electrical connector supplier.

[2] For modules which present a small capacitive load to the host during hot plug (C <= 500nF), the portion of the inrush current due to charging the capacitor can be excluded from the total inrush current which must meet the maximum limit specification.

4.2.5 Grounding

Per specifications given in Ref. [1].

4.3 OPTICAL CHARACTERISTICS

4.3.1 Optical Specifications

The CFP4 module will comply with standardized optical specifications such as the optical reaches specified in IEEE for datacom applications or in ITU-T for telecom applications. Some of the relevant reference documents are: IEEE Std. 802.3™-2012, Telcordia GR-253, ITU-T G.691, ITU-T G.692, ITU-T G.693, and ITU-T G.959, ITU-T G.709.

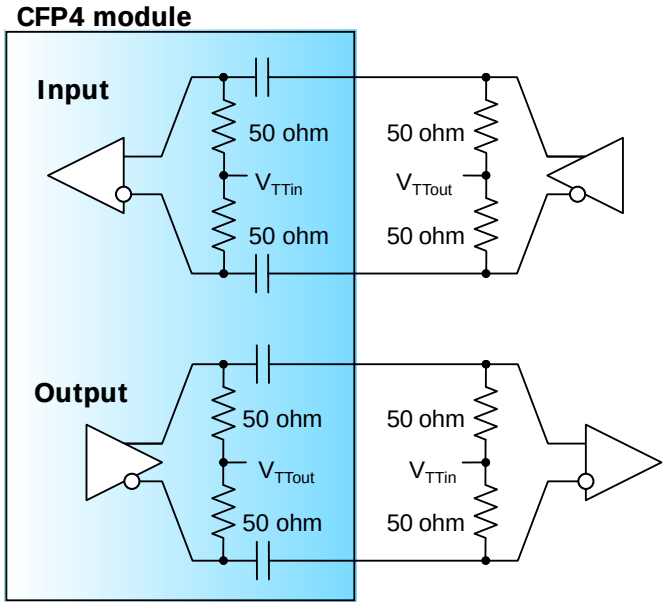
4.4 HIGH SPEED ELECTRICAL CHARACTERISTICS

The CFP4 Module high speed electrical interface supports the following configurations:

1) 4 tx lanes + 4 rx lanes, each at 25 Gbit/s;
2) 4 tx lanes + 4 rx lanes, each at 10 Gbit/s;

The high speed electrical interface shall be AC-coupled within the CFP4 module as is shown in Figure 4-1.

Figure 4-1: High Speed I/O for Data and Clocks



4.4.1 25 Gbit/s Transmitter Data (and Clock)

Per specifications given in Ref. [2].

4.4.2 25 Gbit/s Receiver Data (and Clock)

Per specifications given in Ref. [2].

4.4.3 10 Gbit/s Transmitter Data (and Clock)

The 10 Gbit/s Transmitter Data is defined in IEEE Std. 802.3™-2012 Annex 83A for XLPPI and Annex 83B for XLAUI, or XFI in SFF INF-8077i and SFI in SFF SFF-8431. Figure 4-1 shows the recommended termination for these circuits. Alternate signaling logic are OTL3.4 which are specified in ITU-T Recommendation G.709. Lane orientation and designation is specified in the pin-map tables given in Section 5.

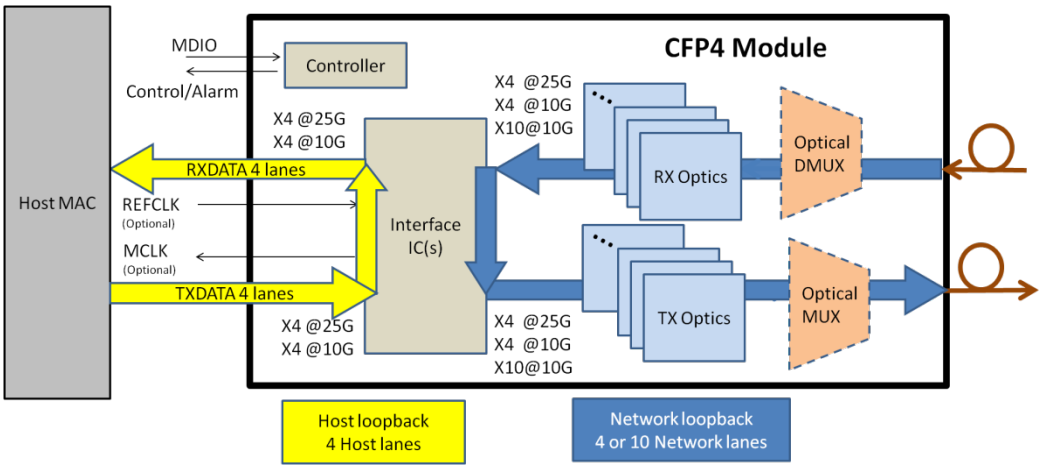
4.4.4 10 Gbit/s Receiver Data (and Clock)

The 10 Gbit/s Transmitter Data is defined in IEEE Std. 802.3™-2012 Annex 83A for XLPPI and Annex 83B for XLAUI, or XFI in SFF INF-8077i and SFI in SFF SFF-8431. Figure 4-1 shows the recommended termination for these circuits. Alternate signaling logic are OTL3.4 which are specified in ITU-T Recommendation G.709. Lane orientation and designation is specified in the pin-map tables given in Section 5.

4.4.5 Loopback (Optional)

The CFP4 module may optionally support loopback functionality. Loopback commands are accessed via the MDIO management interface. Recommended loopback orientation implementation is TX0 to RX0. The host loopback and the network loopback are oriented per Figure 4-2 shown below. The capability to support the loopback functionality is dependent upon the interface IC technology, labeled as “Interface IC(s)” block in the figure. The CFP MSA module vendor will specify which loopback functionality, if any, is supported. For details on controlling the loopback mode, please refer to Ref. [3].

Figure 4-2: CFP4 Module Optional Loopback Orientation


CFP4 Module
Host MAC
MDIO
Control/Alarm
Controller
X4 @25G
X4 @10G
RXDATA 4 lanes
REFCLK
(Optional)
MCLK
(Optional)
TXDATA 4 lanes
X4 @25G
X4 @10G
Interface
IC(s)
X4 @25G
X4 @10G
X10@10G
RX Optics
Optical
DMUX
X4 @25G
X4 @10G
X10@10G
TX Optics
Optical
MUX
Host loopback
4 Host lanes
Network loopback
4 or 10 Network lanes

4.4.6 Reference Clock (Optional)

For 4 x 25 Gbit/s host electrical interface applications, the host may supply a reference clock (REFCLK) at 1/160 electrical lane rate. The CFP4 module may use the 1/160 reference clock for transmitter path retiming, for example for Datacom applications.

The host may optionally supply a reference clock (REFCLK) at 1/40 electrical lane rate for 4 x 25 Gbit/s applications. The CFP4 module may optionally use the 1/40 reference clock for transmitter path retiming, for example for Telecom applications.

For 4 x 10 Gbit/s host electrical interface applications, the host may supply a reference clock (REFCLK) at 1/64 electrical lane rate. The CFP4 module may use the 1/64 reference clock for transmitter path retiming, for example for Datacom applications.

The host may optionally supply a reference clock (REFCLK) at 1/16 electrical lane rate for 4 x 10 Gbit/s applications. The CFP4 module may optionally use the 1/16 reference clock for transmitter path retiming, for example for Telecom applications.

When provided, the REFCLK shall be CML differential AC-coupled and terminated within the CFP4 module as shown in Figure 4-1. There is no required phase relationship between the data lanes and the reference clock, but the clock frequency shall not deviate more than specified in Table 4-2. For detailed clock characteristics please refer to the below table.

Table 4-2: Optional Reference Clock Characteristics

		Min.	Typ.	Max.	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency						See Table 4-4: CFP4 Module Clocking Signals
Frequency Stability	Δf	-100		100	ppm	For Ethernet applications;
		-20		20		For Telecom applications
Input Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
RMS Jitter[1,2]	σ			10	ps	Random Jitter. Over frequency band of 10kHz < f < 10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10/90%	$t_{r/f}$	200		1250	ps	1/160 of electrical lane rate for 4 x 25 Gbit/s and 1/64 of electrical lane rate for 4x 10 Gbit/s
		50		315		1/40 of electrical lane rate for 4 x 25 Gbit/s and 1/16 of electrical lane rate for 4 x 10 Gbit/s

[1] The spectrum of the jitter within this frequency band is undefined. The CFP4 shall meet performance requirements with worst case condition of a single jitter tone of 10ps RMS at any frequency between 10 KHz and 10 MHz.

[2] For Telecom applications better jitter may be required.

An example of CFP4 clocking for 4 x 25 Gbit/s applications is shown in Figure 4-3. An example of CFP4 clocking for 4 x 10 Gbit/s applications is shown in Figure 4-4.

4.4.7 Transmitter Monitor Clock (Optional)

Not specified in this document.

4.4.8 Receiver Monitor Clock (Optional)

Not specified in this document.

4.4.9 Monitor Clock (Optional)

The CFP4 module may supply either a transmitter monitor clock or a receiver monitor clock for 4 x 25 Gbit/s applications. This option is not available for 4 x 10 Gbit/s applications. The monitor clock is intended to be used as a reference for measurements of the optical input or output. If provided, the clock shall operate at a rate relative to the optical network lane rate of 1/8 or 1/32 of 25 Gbit/s. Another option is a clock at 1/40 or 1/160 the rate of (host) transmitter electrical input data for 4 x 25 Gbit/s. Clock termination is shown in Figure 4-1. Detailed clock characteristics are specified in Table 4-3.
The user can select the source of the Monitor clock. MDIO register bits to select the source of the MCLK for CFP4 module is prepared in VR region. Please refer to Ref.[3] for details.

Table 4-3: Optional Monitor Clock Characteristics

		Min.	Typ.	Max.	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency						See Table 4-4: CFP4 Module Clocking Signals
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

Table 4-4: CFP4 Module Clocking Signals

Clock Name	Status	I/O	M x 25 Gbit/s Default Host Lane Rate		Optional Rate
			Datacom 100GBASE-SR4/LR4/ER4 /SR10	**Telecom** OTU4	
REFCLK	*Optional*	I	1/160 (161.1328 MHz) or 1/40 (644.5313 MHz)	1/160 (174.7031 MHz) or 1/40 (698.8123 MHz)	
MCLK	*Optional*	*O*	1/8 (3.22266 GHz) or 1/32 (805.665 MHz) or 1/40 (644.5313 MHz) or 1/160 (161.1328 MHz)	1/8 (3.49406 GHz) or 1/32 (873.515 MHz) or 1/40 (698.8123 MHz) or 1/160 (174.7031 MHz)	
Clock Name	**Status**	**I/O**	**M x 10 Gbit/s Default Host Lane Rate**		**Optional Rate**
			Datacom 40GBASE-SR4/LR4/ER4 40GBASE-FR	**Telecom** OC-768/STM-256,OTU3	
REFCLK	*Optional*	I	1/64 of host lane rate	1/64 of host lane rate	1/16 of host lane rate
MCLK	*Not Available*				

Note: Multi-protocol modules are recommended to adopt the clock rate used in Telecom applications.

Figure 4-3: Example of Clocking for 4 x 25 Gbit/s CFP4 Applications

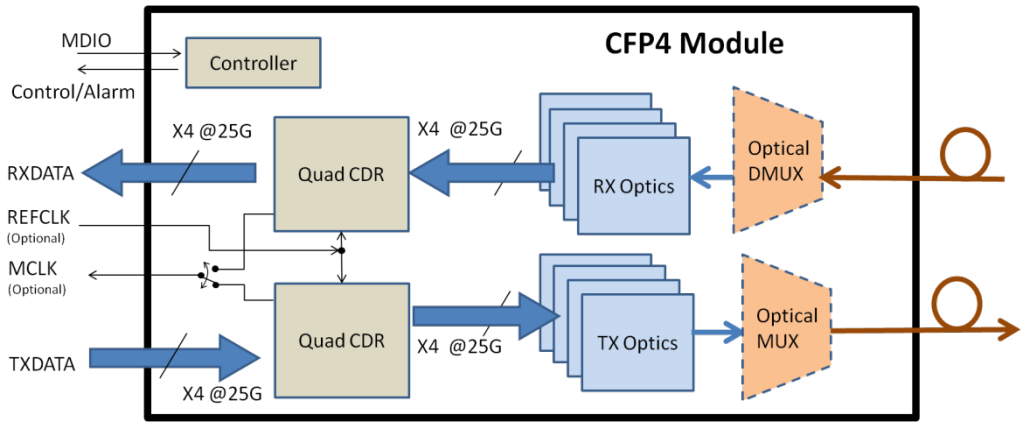
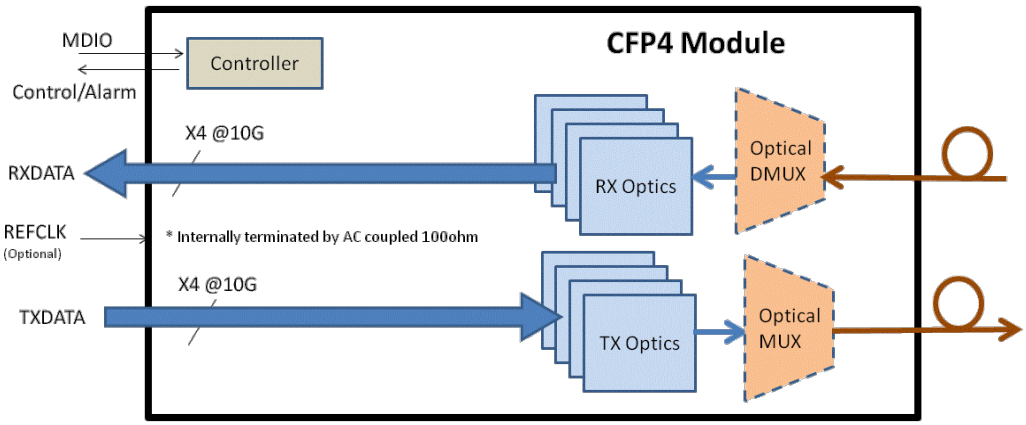


Figure 4-4: Example of Clocking for 4 x 10 Gbit/s CFP4 Applications



5 MECHANICAL SPECIFICATIONS

5.1 Mechanical Overview

The CFP4 module is designed to be plugged into a host cage assembly with a riding heat sink. The cage assembly is fabricated within the host system and the CFP4 module may be inserted at a later time. Shown in Figure 5-1 is a drawing of the CFP4 module and CFP4 modules inserted into a host quad-port cage system with a riding heat sink.

Figure 5-1: CFP4 Module & CFP4 Module Mated in Host Quad Port System

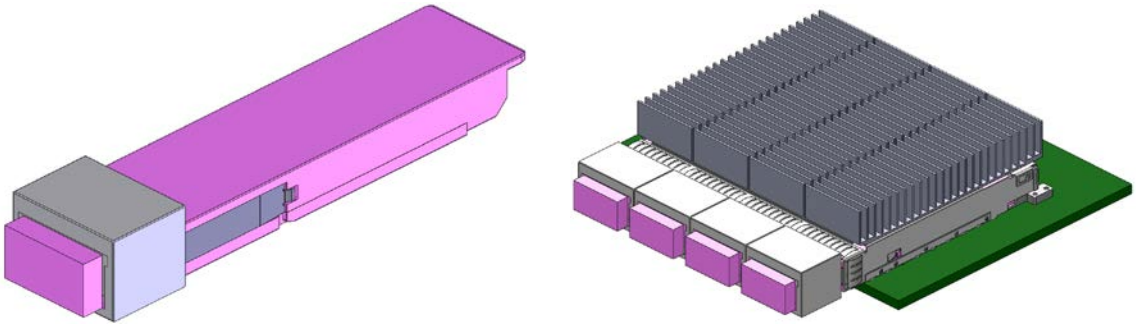
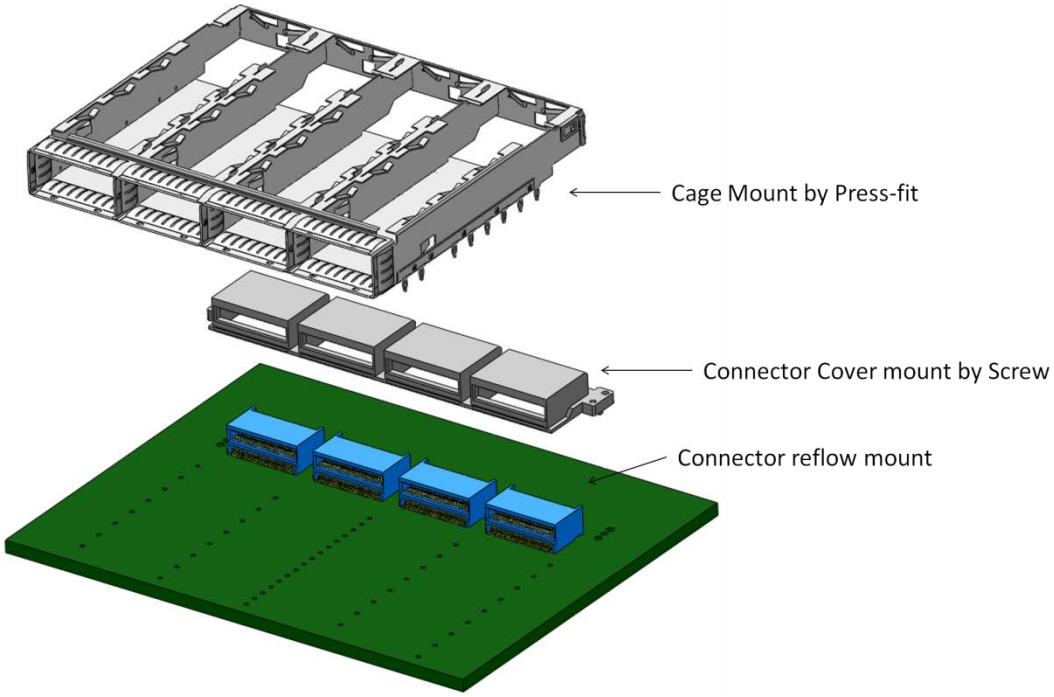


Figure 5-2 is an overview of the CFP4 mechanical assembly the constituent elements. The detailed dimensions are located in a separate design document hosted on the CFP MSA Website (www.cfp-msa.org).

Figure 5-2: Host Cage System and Mounting Method Overview



* Other mounting options are possible.

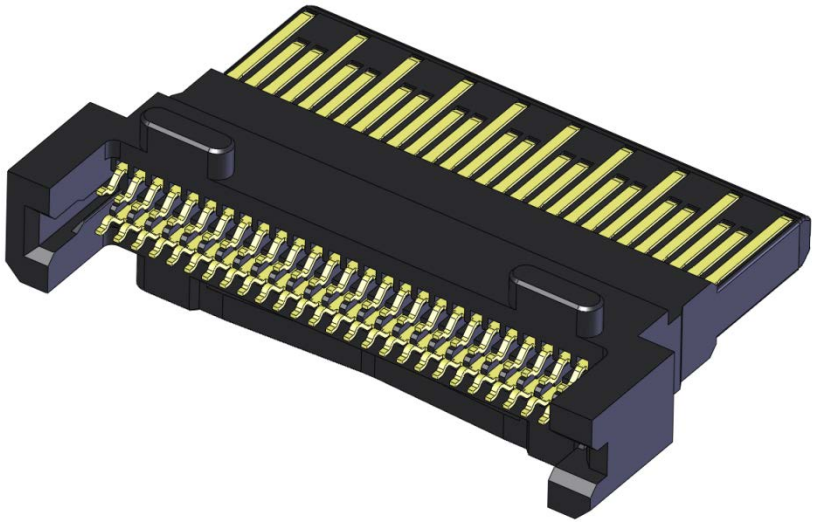
5.2 Electrical Connector

Shown below are details of the electrical connector system used for the CFP4 MSA. The detailed dimensions are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org).

5.2.1 Module Plug Connector

The CFP4 MSA specifies a two piece electrical connector for superior electrical performance and superior mechanical integrity. Shown in Figure 5-3 is the module plug connector assembly which is contained as a sub-component within the CFP4 module.

Figure 5-3: CFP4 Module Plug Connector Assembly



5.2.2 Host Connector

The CFP4 MSA specifies a two piece electrical connector for superior electrical performance and superior mechanical integrity. Shown in Figure 5-4 and Figure 5-5 are overview drawings of the host connector cover and the host connector assembly. These assemblies shall be built into the host system. The Host Connector shall be covered by the Host Connector Cover Assembly.

Figure 5-4: CFP4 Quad Port Host Connector Cover Assembly

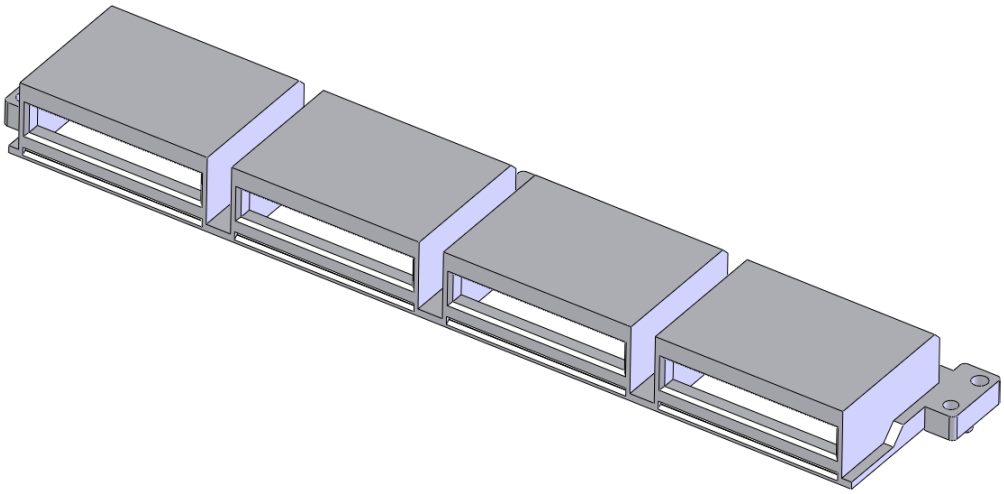
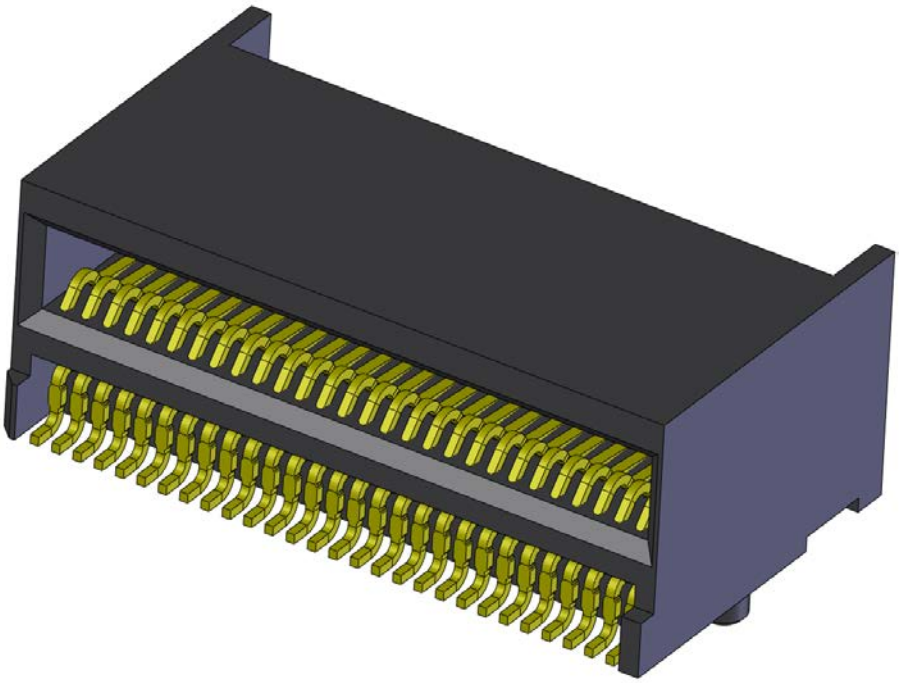


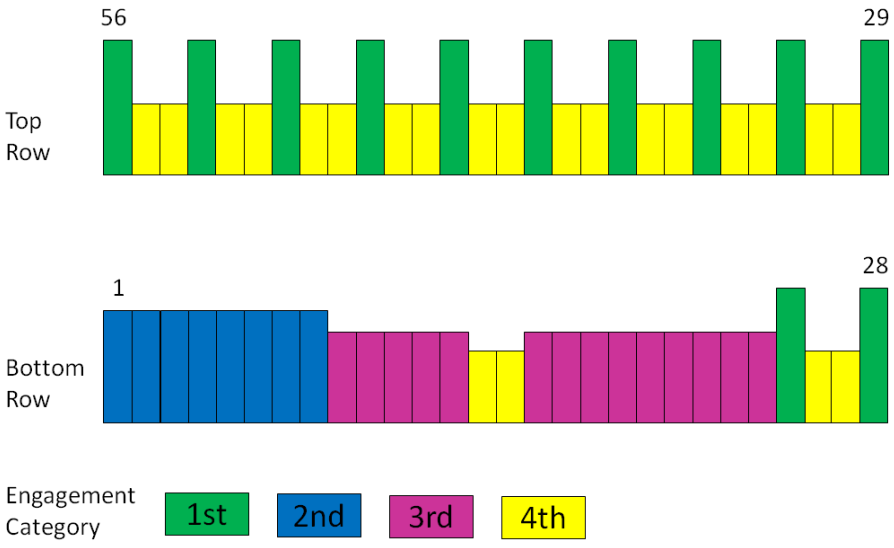
Figure 5-5: CFP4 Host Connector Assembly



5.2.3 Connector Pin Contact Mating

The module plug connector has a physical offset of metal contact pins to insure that certain signals make engagement between the module and host prior to other signals. There are four categories of pin engagement. A map of the connector engagement is shown in Figure 5-6. The connector pin map engagement order is guaranteed by the physical offset built into the module plug connector. The host connector has all contacts on the same plane without offset.

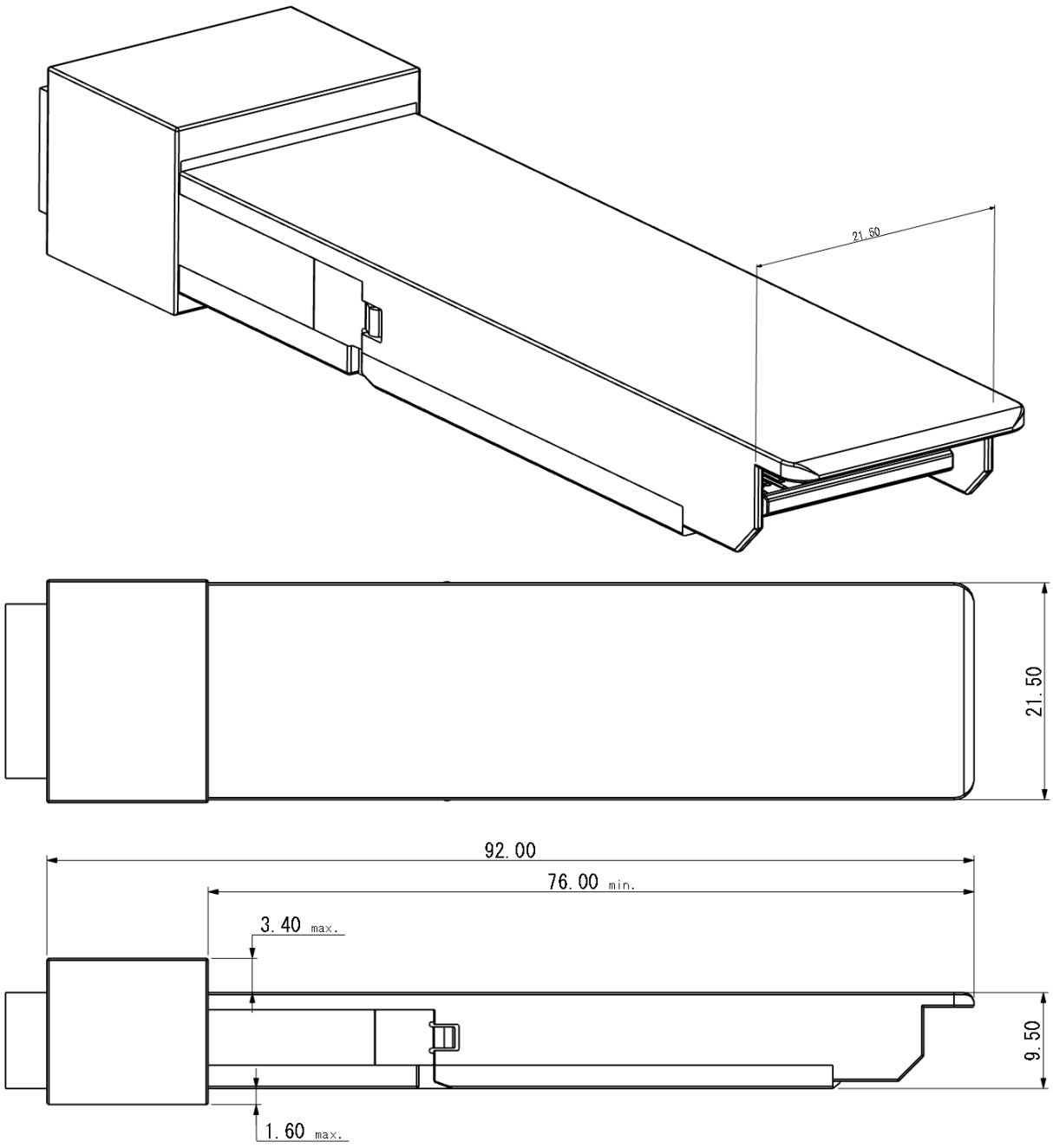
Figure 5-6: CFP4 Pin Map Connector Engagement



5.3 CFP4 Module Dimensions

An overview of the CFP4 module dimensions is show in the below Figure 5-7. The CFP4 maximum header height is specified as shown in Figure 5-7. The detailed CFP4 module dimensions are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org). All mechanical hardware dimensions in this document are for reference only. Normative dimensions are found in the latest published CFP4 baseline drawing.

Figure 5-7: CFP4 Module Dimension Overview



5.3.1 CFP4 Mechanical Surface Characteristics

The mechanical surface of flat top CFP4 module which may be in contact with the host riding heat sink assembly shall be compliant with specifications in Table 5-1. The parameters listed in Table 5-1 define the CFP4 module thermal interface and may be used by host system designers to specify the host cage assembly opening and riding heat sink for optimizing host system thermal management performance. Surface flatness and roughness parameters are specified per CFP4 module power class (see Table 4-1) to allow for optimization of module thermal performance and cost. Non-compliance to these specifications may cause significant thermal performance degradation. Only the top surface of the module is assumed to be used for heat transfer.

Table 5-1: CFP4 Mechanical Characteristics

Parameters	Power Class	Min.	Max.	Unit	Notes
Weight	1 – 6		90	g	
Flatness	1		0.15	mm	
	2		0.15	mm	
	3		0.12	mm	
	4		0.12	mm	
Roughness	1		3.2	Ra	
	2		3.2	Ra	
	3		1.6	Ra	
	4		1.6	Ra	
Temperature Delta	1 - 4		7	°C	No heat sink; 200 lfm sideways airflow
Normal force exerted on module	1 - 4	5	15	N	Heat sink on module top surface

5.3.2 CFP4 Insertion & Extraction

As described in Section 1, the CFP4 module shall be hot pluggable. A consequence of the CFP4 module being hot pluggable is that an end user be equipped to insert and extract the module in the field. The required forces are specified below in Table 5-2.

Table 5-2: CFP4 Module Insertion, Extraction Forces

	Max.	Unit	Notes
Maximum Insertion Force	60	N	Without Heat Sink
Maximum Extraction Force	50	N	Without Heat Sink
Minimum Module Retention Force	90	N	No damage to module below 90 N
Minimum Cage Retention Force	180	N	No damage to cage latch below 180 N

Minimum rating for host/module connector insertion/extraction is 200 cycles.

* Typical increase in those forces by adding heat sink is below 5N.

5.4 Host System Dimensions

The detailed CFP4 host system dimensions including host board layout are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org).

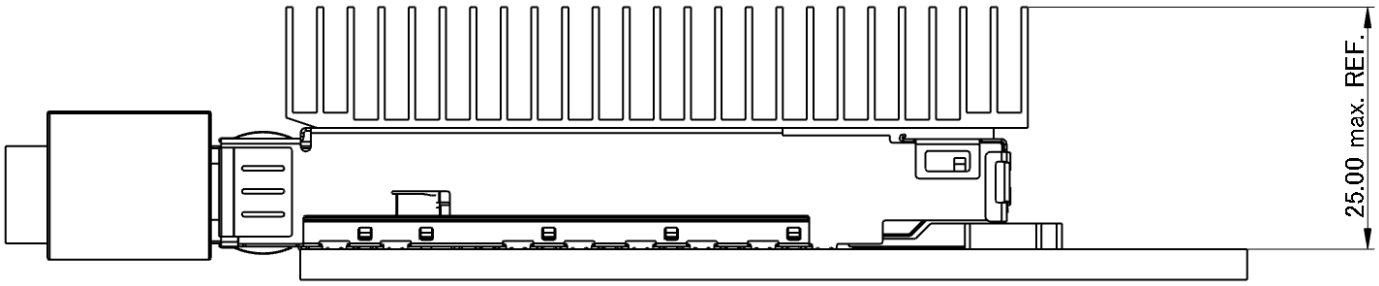
5.5 Riding Heat Sink

The riding heat sink and host cage top surface designs given in the latest published CFP4 baseline drawing are

only exemplary and are not required for compliance with the CFP4 MSA. Cage opening and heat sink specifications vary with host system design and thermal performance requirements. The heat sink/cage designs are therefore host system dependent and may be optimized by the system designer.

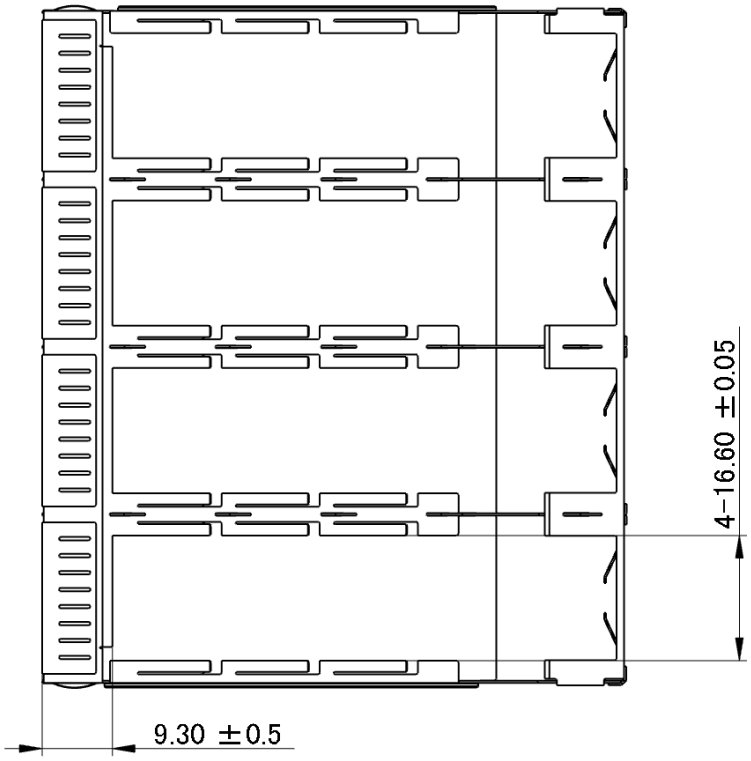
The riding heat sink illustrated in Figure 5-8 is for example only. The recommended material for the heat sink is aluminum.

Figure 5-8: Riding Heat Sink



The mounting dimensions for the Riding Heat Sink are shown below in Figure 5-9. The actual dimensions of the heat sink and cage top opening may be optimized for the particular host system.

Figure 5-9: Host Cage Top Surface Opening



5.6 Optical Connectors

The CFP4 module shall support LC, MTP12 and MTP24 optical connector types, as listed in Table 5-3.

Table 5-3: Optical Connectors[3]

Pin #	Category	Reference Number
LC Connector	TBA	TBA
MPO12 Connector	TBA	TBA
MPO24 Connector	TBA	TBA

5.6.1 Optional Optical LC Connector Position for Telecom Applications

Not supported in the CFP4 module.

[3] Other optical connectors may be supported

5.7 Electrical Connectors

CFP4 host electrical connector supplier information will be added to Table 5-4 in a future release of this MSA.

Table 5-4: CFP4 Host Connector Assembly

Part Number	Supplier	Part Name
TBA	TBA	Cage
TBA	TBA	Host Connector Cover Assembly
TBA	TBA	Host Connector

5.8 Pin Assignment

The CFP4 connector has 56 pins which are arranged in Top and Bottom rows. The CFP4 connector supports the following configurations:

Four (4) 25Gbit/s TX lanes plus four (4) 25Gbit/s RX lanes;

The CFP4 pin-orderings are shown in Table 5-5. The CFP4 TOP pin-out definition uses the same pin-ordering convention as CFP and CFP2. There is also an optional CFP4 TOP ALT1 pin-out definition which follows the QSFP pin-ordering convention. All modules must support the baseline TOP pin-out definition. The optional TOP ALT1 pin-definition can be switched to after power-up by using MDIO commands to switch the pin-ordering. For details, please refer to “CFP MSA Management Interface Specification”

Detailed description of the bottom row pins 1 through pin 28 are given in Table 5-6. Note the REFCLK pins are located on the top row along with the high-speed TX and RX data pins. A single-ended REFCLK is an option. The CFP4 connector pin map orientation is shown in Figure 5-10.

Figure 5-10: CFP4 Connector Pin Map Orientation

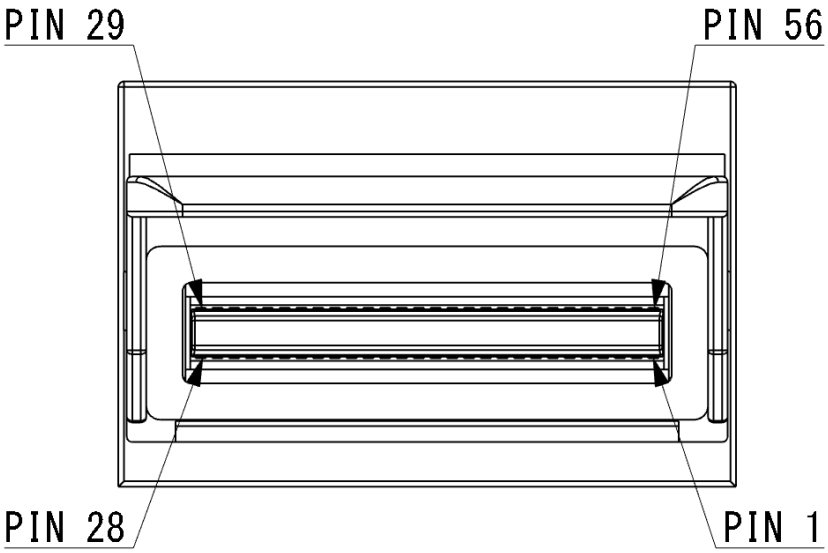

PIN 29
PIN 56
PIN 28
PIN 1

Table 5-5: CFP4 4x25Gbit/s Pin Map

Pin view from top ==> Host

	CFP4 Bottom		CFP4 Top	CFP4 Top ALT1
1	3.3V_GND	56	GND	GND
2	3.3V_GND	55	TX3n	TX0n
3	3.3V	54	TX3p	TX0p
4	3.3V	53	GND	GND
5	3.3V	52	TX2n	TX1n
6	3.3V	51	TX2p	TX1p
7	3.3V_GND	50	GND	GND
8	3.3V_GND	49	TX1n	TX2n
9	VND_IO_A	48	TX1p	TX2p
10	VND_IO_B	47	GND	GND
11	TX_DIS *(PRG_CNTL1)*	46	TX0n	TX3n
12	RX_LOS *(PRG_ALRM1)*	45	TX0p	TX3p
13	GLB_ALRMn	44	GND	GND
14	MOD_LOPWR	43	*(REFCLKn)*	*(REFCLKn)*
15	MOD_ABS	42	*(REFCLKp)*	*(REFCLKp)*
16	MOD_RSTn	41	GND	GND
17	MDC	40	RX3n	RX3p
18	MDIO	39	RX3p	RX3n
19	PRTADR0	38	GND	GND
20	PRTADR1	37	RX2n	RX2p
21	PRTADR2	36	RX2p	RX2n
22	VND_IO_C	35	GND	GND
23	VND_IO_D	34	RX1n	RX1p
24	VND_IO_E	33	RX1p	RX1n
25	GND	32	GND	GND
26	*(MCLKn)*	31	RX0n	RX0p
27	*(MCLKp)*	30	RX0p	RX0n
28	GND	29	GND	GND

REFCLK
(Optional)

MCLK = TX_MCLK + RX_MCLK
(Optional)

TX_DIS *(PRG_CNTL1)*
(Optionally configurable as Progammable Control after Reset)

RX_LOS *(PRG_ALRM1)*
(Optionally configurable as Progammable Alarm after Reset)

Table 5-6: CFP4 Bottom Row Pin Description for 4 x 25 Gbit/s Applications

PIN #	NAME	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
3	3.3V			3.3V Module Supply Voltage
4	3.3V			3.3V Module Supply Voltage
5	3.3V			3.3V Module Supply Voltage
6	3.3V			3.3V Module Supply Voltage
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
9	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect
10	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect
11	TX_DIS *(PRG_CNTL1)*	I	LVCMOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled (Optionally configurable as Programmable Control1 after Reset)
12	RX_LOS *(PRG_ALRM1)*	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition (Optionally configurable as Programmable Alarm1 after Reset)
13	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
14	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
15	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
16	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
17	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
18	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010)
19	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
20	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
21	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
22	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
23	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect
24	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect
25	GND			
26	*(MCLKn)*	O	CML	For optical waveform testing. Not for normal use.
27	*(MCLKp)*	O	CML	For optical waveform testing. Not for normal use.
28	GND			

5.9 CFP4 Bail Latch Color Coding and Labeling

The CFP4 module bail latch color is used to indicate module optics application. The CFP4 bail latch color code scheme is specified in Table 5-7.

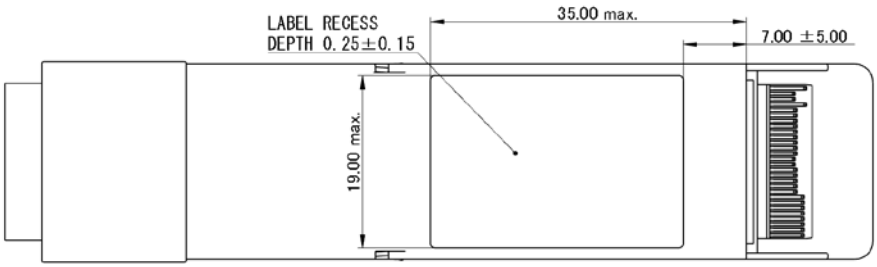
Table 5-7: CFP4 Bail Latch Color Coding

Bail Latch Color Minimum reach & Minimum loss	**Bail Latch Band**			
	10G/fiber One center black band (010)	25G/fiber (or 20G/fiber) Two side black bands (101)	50G/fiber (or 40G/fiber) Three black bands (111)	100G/fiber No bands (solid color) (000)
Beige 100m & 2dB (MMF)	100GE-SR10 Mx 40GE-SR4 Nx 10GE-SR	100GE-SR4	Mx “40GE-SR”*	“100GE-SR”*
Yellow 500m & 2.5dB (SMF)	“40GE-nR4”* parallel	“100GE-nR4”* parallel	“100GE-nR2”* parallel	“100GE-nR4”*
Green 2km & 4dB (SMF)		“100GE-FR4”* parallel	Mx 40GE-FR	“100GE-FR4”*
Lighter Blue 10km & 6dB	Nx 10GE-LR		Mx 40GE-LR4	100GE-LR4
Lighter Red 30km/40km	Nx 10GE-ER	100G DD DWDM	Mx 40GE-ER4	100GE-ER4
White ≤ 80km	Nx “10GE-ZR”*	100G DD DWDM	Mx “40GE-ZR4”*	“100GE-ZR4”* 100G Coh. DWDM

Note 1: Link budget = Minimum penalty [function of minimum reach] + minimum loss
Note 2: * For potential future application; Not currently a standard nor MSA.
Note 3: Bail latch without any color (including no black bands; metal only) indicates a module that does not fit into any of the defined categories.

The CFP4 module should be clearly labeled. The complete labeling need not be visible when the CFP4 module is installed in the host cage assembly. A recessed area on the bottom of the CFP4 module, as shown in Figure 5-11, is the recommended location for module label.

Figure 5-11: CFP4 Module Label Recess



6 REGULATORY COMPLIANCE

Per specifications given in Ref. [1].

End of Document